63-2-3

INTERIM RESEARCH REPORT NO. 14A

PROJECT

lightning

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Prepared for **DEPARTMENT OF THE NAVY**
Bureau of Ships, Washington 25, D.C.

Prepared by **RADIO CORPORATION OF AMERICA**
Camden, New Jersey

Copy No. 117

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for

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Project LIGHTNING

This report covers the period of
March 1, 1962 to May 31, 1962

Prepared for
DEPARTMENT OF THE NAVY
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Prepared by
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Electronic Data Processing
RADIO CORPORATION OF AMERICA
Camden, New Jersey

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Chapter 1. GENERAL

1-1 INTRODUCTION

In this period fabrication of both the Logic and Memory Subsystems was completed. Both systems were made individually operational. Specifically:

1. Devices

   (a) All devices required for the Logic and Memory Subsystems were delivered.

   (b) Preliminary work on improved and new devices was started. This work is oriented towards improved device characteristics, miniaturization and reduced cost.

2. Logic Subsystem

   (a) The Logic Subsystem is operating as designed.

   (b) The time required to perform a complete cycle of all wired-in instructions is 140 nanoseconds, and is determined by the fixed delay corresponding to the worst-case design times. It has been determined that the actual delays are no greater than one-half the worst-case computed delays.

   (c) There have been a minimum of failures with the prime cause of failures due to poor soldering.

3. Memory Subsystem

   (a) The 32-word Memory Subsystem is undergoing final test.

   (b) All words have been selected at a 33-megacycle rate.

   (c) The extensibility lines incorporating 24 bits have been built and are currently being installed in the nine-word system.

1-2 INTERPRETIVE SUMMARY

The ultimate goal of this project is the construction and operation of the combined Logic-Memory Subsystem. At the end of this period, both the Logic and Memory Subsystems have been built and are operating separately.

A. GENERAL

Upon completion of the Logic Subsystem, fabrication effort was concentrated on the memory peripheral equipment. As a result, the memory and its associated equipment is at an earlier stage of checkout and debugging. Effort is being concentrated in this area in order to insure a smooth transition into the logic-memory combination phase.

B. TUNNELING DEVICES AND COMPONENTS

Tunneling devices and components required for the Memory and Logic Subsystems were delivered, together with a small quantity of spare units. Device fabrication has reached the stage where units whose construction could be made only with great difficulty at the beginning, can now be built in quantity by factory personnel. Development work on improved devices already points the way to better electrical and mechanical characteristics.

C. LOGIC SUBSYSTEM

Complete debugging of the entire Logic Subsystem has been complete for about a month and this setup is being run to provide reliability data. The subsystem was designed using worst-case analysis, and as such, its calculated repetition rate for the full cycle of logical performance was approximately 140 nanoseconds.

Since the systems organization for this machine is asychronous, its repetition rate is limited by fixed delays which are again dependent upon worst-case analysis. Actual measurements of delays on the equipment has failed to show any place in the circuits where the delay is greater than one-half that of the design. Therefore, full cycle time could be reduced to 70 nanoseconds only by modifying the fixed delays.

Since the organization is asychronous, there is no clock as such; therefore, it is difficult to define the resultant action in terms of clock rate. However, the rate of logical operation is considered analogous and there is an effective clock rate. At the present time it is about 60 megacycles. If the delays were modified, the clock rate of this machine could be 120 megacycles.

Tabulated data showing cause of failures has indicated two sources: The most common source has been failure of solder joints. The second is diode failure. It is our belief that those diodes which have failed were early units fabricated by rather primitive methods.

One feature not promised in the proposal for Phase III-B is the ability to operate a continuous ring shift on the accumulator register. It is possible to ring shift this register at an actual rate of 135 megacycles.

D. MEMORY

The 32-word, 5-bit memory stack was completed along with all of the peripheral equipment. A total of 160 bits of this stack have held information without errors for periods up to 3 hours. Due to continual debugging, the equipment reliability is constantly improving with the major causes of intermittance being those associated with mechanical rather than electrical sources. All words have been selected at a 33-megacycle rate operating continuously.

The present decoder, which is built to simulate decoding one out of 1024 locations, requires a total of 30 nanoseconds. This decoder has operated for up to 7 hours at a run.

The read and write registers and the clear inhibit sense amplifier frames required to effect combining the Logic and Memory Subsystem have been built and are now under test.

The nine-word system was demonstrated with locations operating at a cycle time of 15 nanoseconds or a repetition rate of 65 megacycles. Following this demonstration, the repetition rate was decreased somewhat and one of the planes was removed so that its location could accept the 24-bit extensibility word plane. This plane is now under test.

1-3 OBJECTIVES AND SCHEDULES

The combining of the Logic and Memory Subsystems will be completed in the following quarter. This will be done in the following steps:

(a) Mechanically combine the subsystem.

(b) Attach the timing generator for the memory to the logic control console.

(c) Perform individual tests on the Logic and Memory Subsystems operating in a closed loop.

(d) Operate these at full design speeds.

(e) Perform single-step and full-speed operation with all memory locations sequentially storing all word combinations.

At this point, the combined Logic and Memory Subsystem will be complete and operating as an integrated unit.

Chapter 2. LOGIC SUBSYSTEM

SUMMARY

The entire Logic Subsystem has been assembled and tested, and is presently being life tested to obtain reliability data.

All peripheral circuits for the memory have been built and completely tested with the exception of read and write registers and clear inhibit sense amplifier frames which are now under test.

New wafer fabrication methods are being investigated from the viewpoints of size reduction and part replaceability.

Several points of concern in the present fabrication technique are being investigated in order to increase reliability in future machines.

Chapter 2. LOGIC SUBSYSTEM

I. PERSONNEL

The following personnel contributed to this phase of the project during the fourteenth quarter:

F. Borgini
R. J. Fradette
J. W. Harmon
R. J. Linhardt
J. P. Mc Allister
J. L. Miller
H. V. Rangachar
D. E. Roop

II. DISCUSSION

A. LOGIC SUBSYSTEM OPERATION

Operation of the entire Logic Subsystem, shown in Figure 2-1, was realized during this quarter.

Before each unit was installed in the main frame, all diode characteristics and external signal wiring leads were thoroughly checked and all necessary repairs were made.

The first units to be installed into the main frame were controls #1 and #2, parity checkers #1 and #2 and the X register. After these were installed, the power supply was turned on and a running time meter was used to record the number of hours of testing time.

A log was started of all failures encountered during the testing. A summarization of this log with respect to hours of operation is given in Table 2-1. The first 46 hours of operation was associated with checking out of the first five units. At 46 hours, the error counter was inserted in the main frame and at 92 hours, the A register was installed in the main frame. When the A register was inserted, problems were encountered and corrected with the power supply as explained elsewhere in this report. The Logic Subsystem was completely operational at 113 hours of elapsed running time. The total running time at the present writing is 280 hours.

There are three modes of operation which can satisfactorily test the working conditions of all the wafers in the subsystem. These modes are (1) $\overline{\text{INT}}$, $\overline{\text{STEP}}$, REP; (2) INT, $\overline{\text{STEP}}$, $\overline{\text{REP}}$; and (3) $\overline{\text{INT}}$, STEP, REP.

Figure 2-1. Logic Subsystem

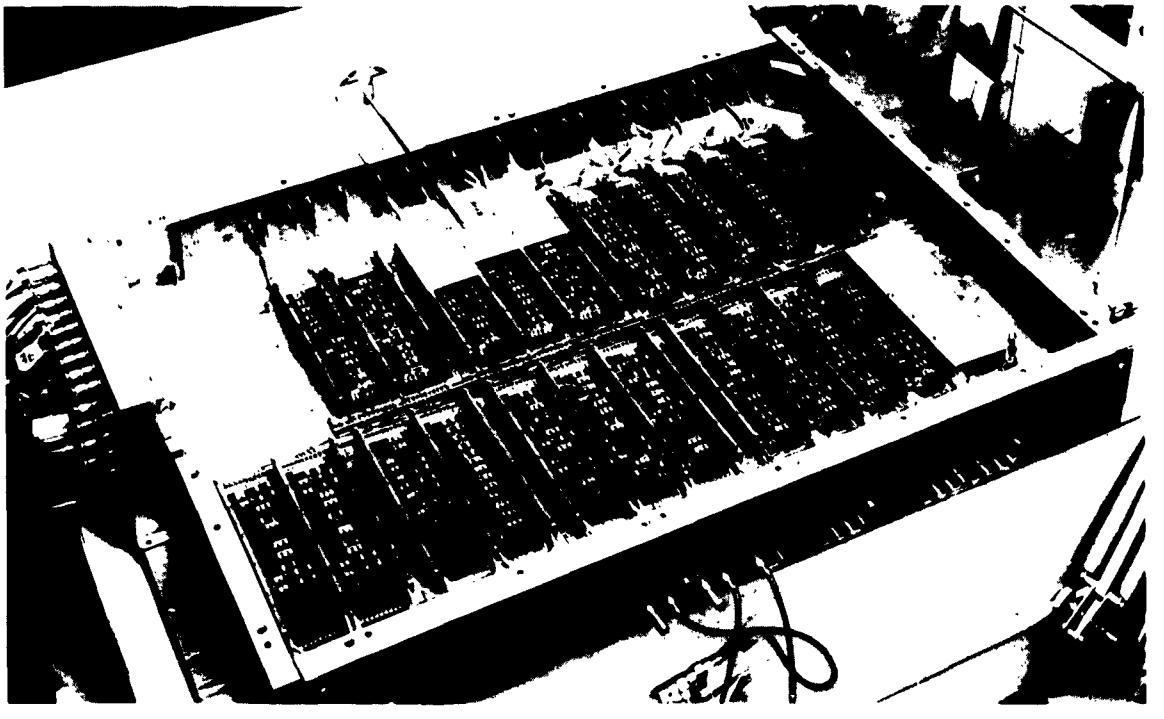


Figure 2-1a. Close-up of Logic Subsystem

TABLE 2-1
SUMMARY OF REPAIRS IN LOGIC SUBSYSTEM

Hours of Operation	Type and Location of Failure	Repair Required
1 hour	Parity Checker #2 AND 3-V was not working because of poor solder connection on 20 ma. T. D.	Resolder T. D.
1 hour	Parity Checker #2 Delay 8-V inv. portion not switching; input to wafer to small.	Increased output of wafer driving 8-V by increasing inductance of output stage.
5 hours	Control #2 OR 10-R output diode developed poor solder connection.	Resoldered diode
10 hours	Control #2 OR 2-T intermittent operation due to poor connection of inductance on 1st stage.	Resoldered inductor
21 hours	Control #2 AND 7-S output diode bad.	Replaced diode
28 hours	Control #2 OR 2-T input diode developed poor solder connection.	Resolder diode
46 hours	Insertion of error counter	
54 hours	Control #1 OR 14-F operation intermitten. Clamp in 2nd stage intermittent.	Replaced clamp diode
61 hours	Error Counter Bis. 2-Y would not set. Clamp in inv. stage was open.	Replace clamp diode
62 hours	Error Counter AND S-W intermittent operation; +6V to 3rd stage intermittent.	Resolder power connection
67. 5 hours	Error Counter Bis. 2-Y would not reset due to poor solder connection in inv. portion.	Resolder connection
74. 1 hours	Error Counter Bis. 2-Y would not reset because of high value 81. 6 ohm resistor.	Replaced resistor

TABLE 2-1
SUMMARY OF REPAIRS IN LOGIC SUBSYSTEM (Continued)

Hours of Operation	Type of Location of Failure	Repair Required
77.4 hours	X Register Bis. 11-F would not set from console because of bad connection to 210 ohm resistor.	Resoldered connection
80 hours	Parity Checker #2 Delay 8-V operation of inverter portion was erratic. AND diode in inverter was bad.	Replaced diode.
85 hours	Control #1 Bis. 8-G would not reset - 25 ma T.D. in inverter driver, bad.	Replaced 25 ma T.D.
91.5 hours	Control #1 Bis. 8-G would not reset because of spurious signals being produced by large coil in output to console.	Increased isolation between the wafer and console with series resistor.
94.5 hours	A register inserted in main frame	
100.0 hours	A Register Bis. 7-E Set amplifier oscillating — 25 ma T.D. bad.	Replaced T.D.
102 hours	X Register Bis. 11-N was not resetting inverter pulse not wide enough.	Increased inductance in inverter.
103 hours	X Register Bis. 11-N would not transfer X3 ⟶ A2 output; OR diode was open.	Replaced diode
106.3 hours	X Register AND 7-Q 2nd stage oscillating -20 ma T.D. bad.	Replaced 20 ma T.D.
110.0 hours	Parity Checker #1 Delay 2-K not operating; Clamp on output stage not soldered	Resolder clamp
114 hours	Error Counter AND 6-W not working because of high value (22.7 ohms) input resistor.	Replaced 22.7 ohms resistor.

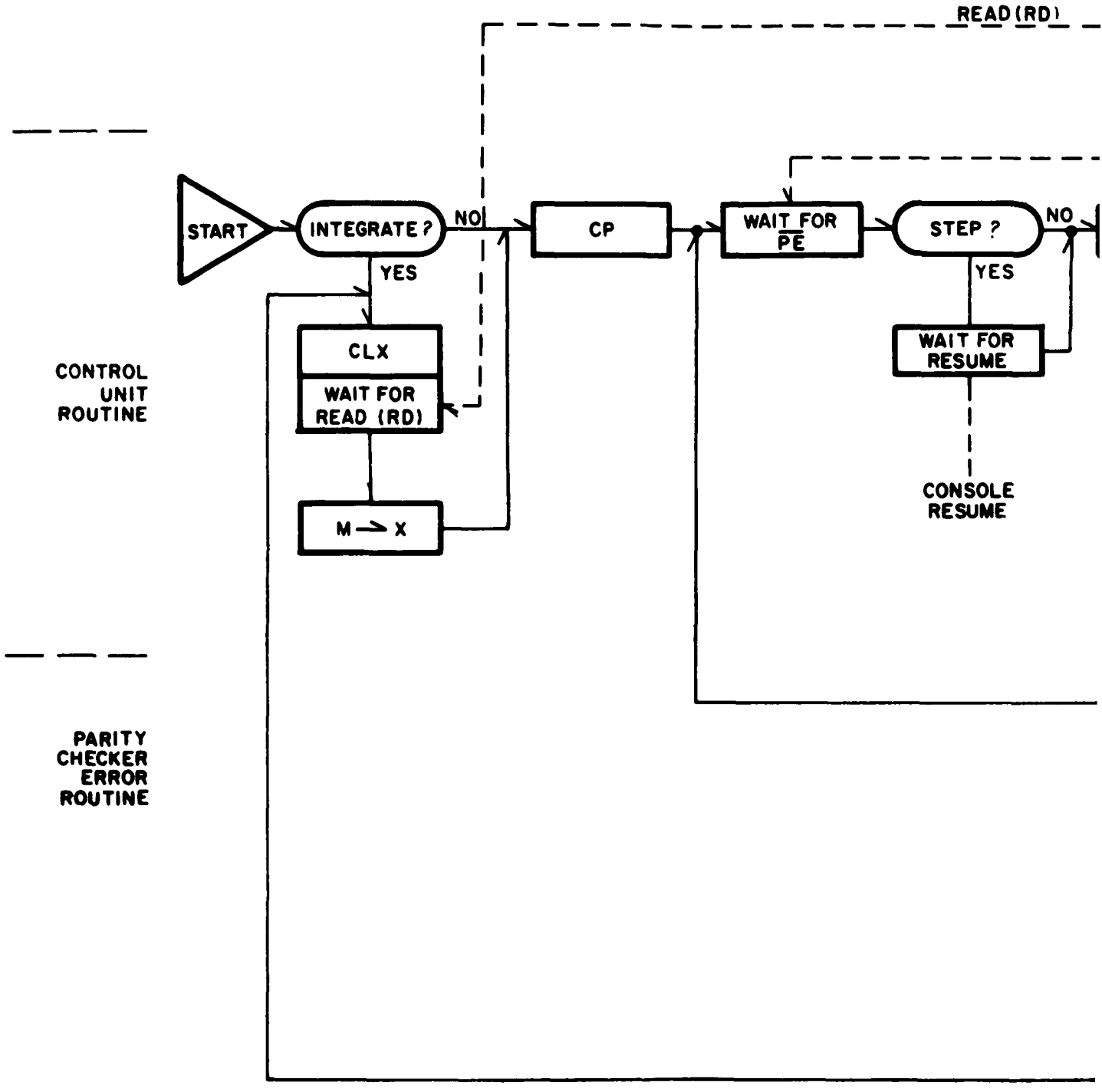
TABLE 2-1
SUMMARY OF REPAIRS IN LOGIC SUBSYSTEM (Continued)

Hours of Operation	Type of Location Failure	Repair Required
127.5 hours	X Register Bis. 10-M would not reset because 50 ma T. D. in bistable portion developed bad connection.	Resoldered 50 ma T. D.
148.6 hours	Control #1 Bis. 8-G would not reset due to poor solder connection in inverter.	Resoldered connection
200.5 hours	X Register Bis. 13-P would not set because clamp was open in inverter stage.	Replaced clamp diode

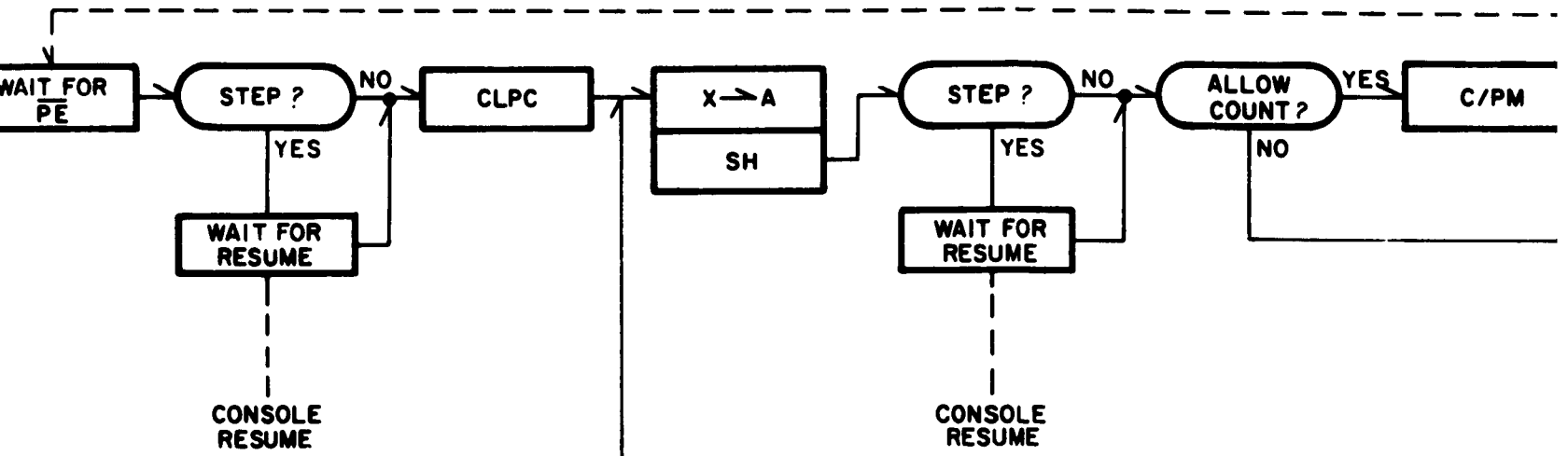
These three modes are set up from the console by selecting the appropriate switches which provide the d-c levels on AND gates necessary for the operation of the selected routine. The $\overline{\text{INT}}$, STEP, REP mode proceeds through the subsystem one step at a time as shown in Figure 2-2. The $\overline{\text{INT}}$, $\overline{\text{STEP}}$, REP mode operates the same as the mode above except that it runs on itself once it is started. The third mode (INT, $\overline{\text{STEP}}$, $\overline{\text{REP}}$) as now used simulates operation in combination with the memory.

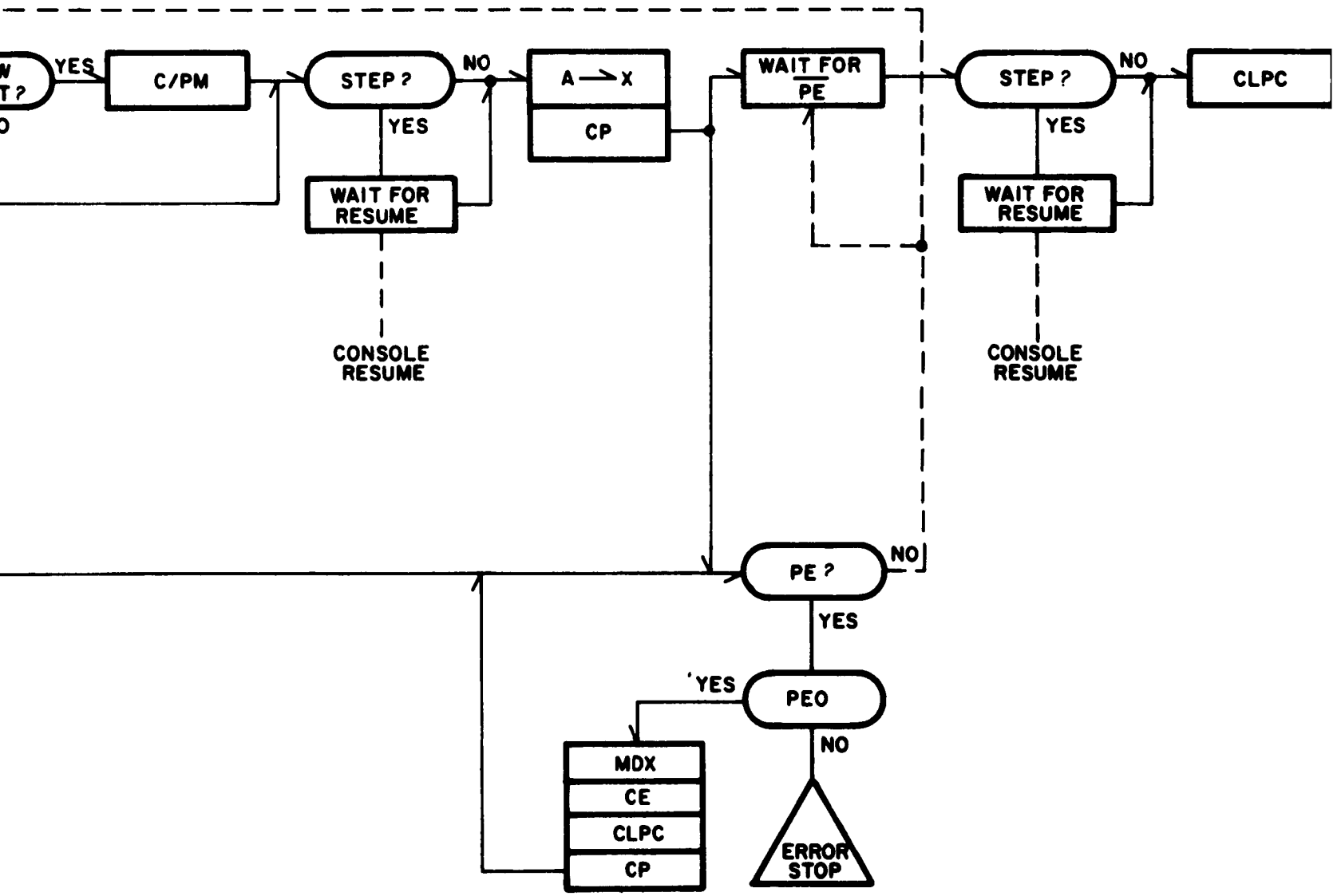
Permissable supply voltage variations (before malfunction) were checked in all 3 operating modes and typical values are listed in Table 2-2. These values were obtained by varying one voltage while holding the others at nominal.

Delay time measurements were made in the Logic Subsystem. Table 2-3 shows the measured time between commands from the control unit as compared to the actual time necessary to complete a specific instruction. In all instances the delays provided in the control unit are approximately 2 times larger than actual operation times. Photographs of these delays are shown in Figure 2-3. Similar measurements were made in the parity checker with results given in Table 2-4. The ratio here between circuit operation time and program delay time is greater than 2 to 1. Photographs of these delays are shown in Figure 2-4, indicating the time necessary for the bistable circuits in each level to be reset, thereby dictating the time in which a $\overline{\text{PE}}$ signal can be received. The photographs clearly indicate that parity could be checked in 22.5 nanoseconds, but because the worst-case delays are provided for, it now takes 65 nanoseconds.


READ (RD)
START
INTEGRATE ?
NO
YES
CP
WAIT FOR PE
STEP ?
NO
YES
CLX
WAIT FOR READ (RD)
M → X
WAIT FOR RESUME
CONSOLE RESUME
CONTROL UNIT ROUTINE
PARITY CHECKER ERROR ROUTINE

READ(RD)


WAIT FOR PE
STEP ?
NO
YES
WAIT FOR RESUME
CONSOLE RESUME
CLPC
X→A
SH
STEP ?
NO
YES
WAIT FOR RESUME
CONSOLE RESUME
ALLOW COUNT?
YES
NO
C/PM


YES
C/PM
STEP ?
NO
YES
WAIT FOR RESUME
CONSOLE RESUME
A → X
CP
WAIT FOR PE
STEP ?
NO
CLPC
YES
WAIT FOR RESUME
CONSOLE RESUME
PE ?
NO
YES
YES
PEO
NO
MDX
CE
CLPC
CP
ERROR STOP

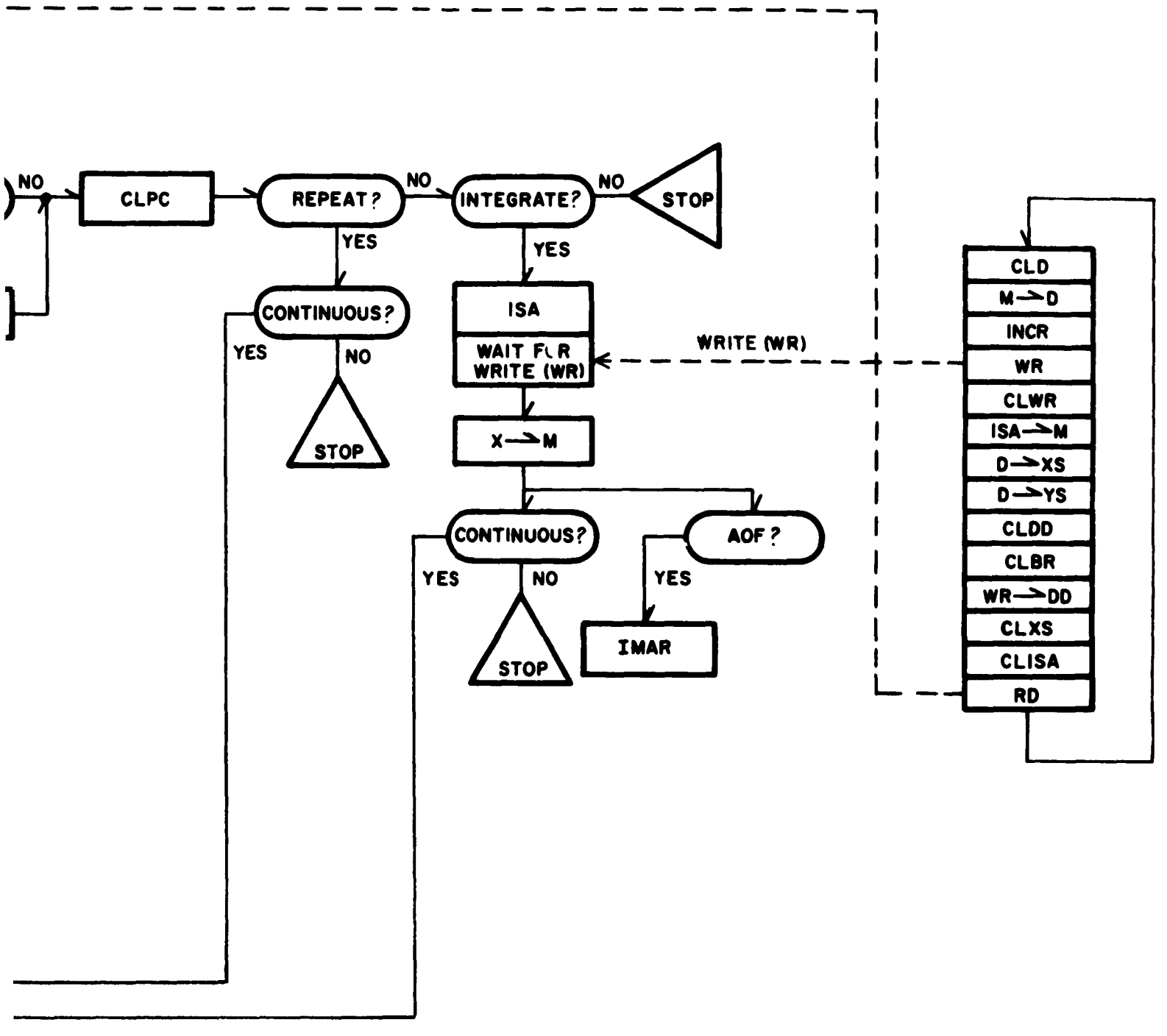


Figure 2-2. LIGHTNING Subsystem Control Routine

TABLE 2-2
POWER SUPPLY VOLTAGE VARIATIONS FOR THE 3 MODES OF OPERATION

Mode of Operation	POWER SUPPLY VOLTAGES		
	+90mv (ΔMV)	+6.0V (ΔMV)	*-6.0V (ΔMV)
$\overline{INT}$, $\overline{STEP}$, REP	-28	-160	-450
	+18	+130	+250
INT, $\overline{STEP}$, $\overline{REP}$	-20	-120	-600
	+15	+130	+250
$\overline{INT}$, STEP REP	-30	-150	-600
	+18	+100	+250

* The -6.0 volts was only raised 250 MV to avoid greatly exceeding the wattage rating of the 81.6-ohm resistors.

From the data taken thus far, a comparison can be made between the best-and worst-case conditions of the Logic Subsystem based on the following assumptions:

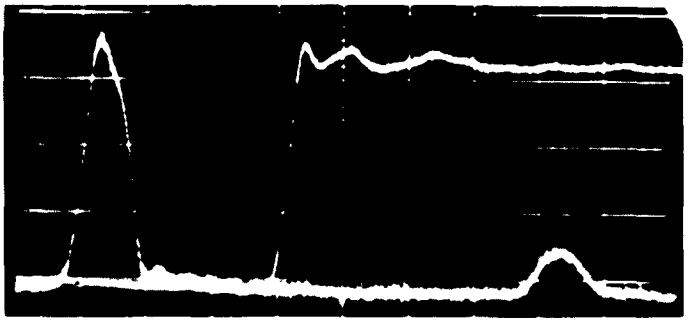
AND Wafer	1.1 - 2.0 (MS)
OR Wafer	0.9 - 1.4 (MS)
Bistable wafer	Set 0.7 - 4.1 (MS)
	Reset 0.7 - 4.1 (MS)
Delay wafers	±10%
ns Wire Delay	Length (in)/8

Table 2-5 shows values actually obtained in measurements made in the Logic Subsystem.

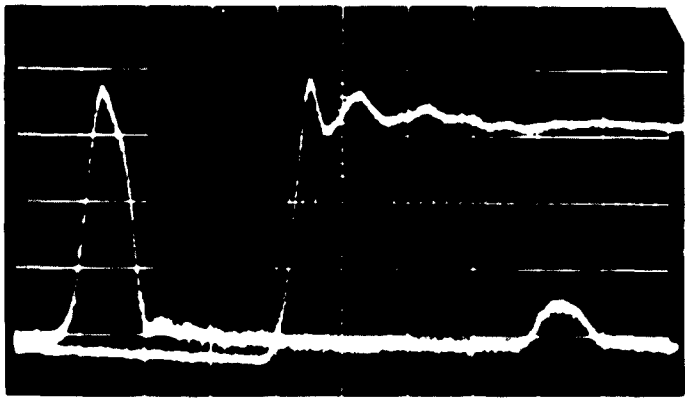
A comparison has been made in Table 2-6 of the earliest and latest time of control unit outputs to actual measured times. In this Table X→A has been used as the reference.

TABLE 2-3
TRANSIT TIME MEASUREMENTS FOR LOGIC ROUTINE

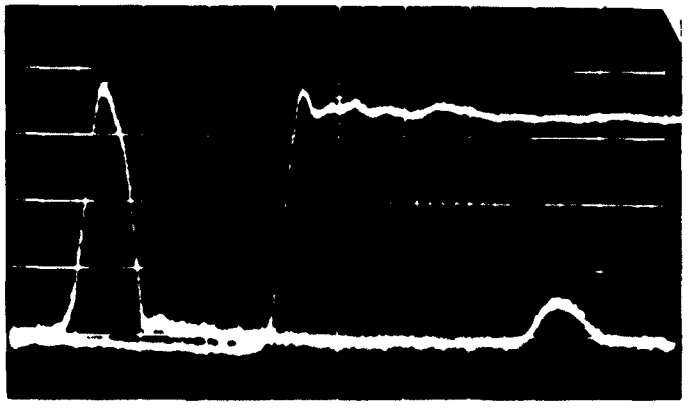
Command	Time to Complete Instruction (NS)	Time to Next Instruction (NS)	Bit Observed in Transfer or Shift
X⟶A	7.5	15	$X_o \longrightarrow A_3$
SHIFT	7.0	14	$A_3 \longrightarrow A_o$
COUNT (Same Time)	5.7(1st bit) 12(4th bit)	25.2	1st & 4th bit in A-REG.
PM (Same Time)	7.1	25.2	Parity bit in A-REG.
A⟶X	5.7	12.4	1st bit in X-REG.
CP	65		
X⟶A	7.2	15	$X_1 \longrightarrow A_o$
SHIFT	6.4	14	$A_o \longrightarrow A_1$
X⟶A	7.0	15	$X_2 \longrightarrow A_1$
SHIFT	6.4	14	$A_1 \longrightarrow A_2$
X⟶A	6.8	15	$X_3 \longrightarrow A_2$
SHIFT	6.1	14	$A_2 \longrightarrow A_3$
A⟶X	6.0	12.4	$A_1 \longrightarrow X_1$
A⟶X	5.5	12.4	$A_2 \longrightarrow X_2$
A⟶X	5.8	12.4	$A_3 \longrightarrow X_3$
A⟶X	4.8	12.4	$A_4 \longrightarrow X_4$
CL. PC.	4.2 (best case)		13-G⟶10K (3⊕)
CL. PC.	5.0 (worst case)		13-G - -⟶6V (1⊕)
CL⟶X	3.6		4R⟶4P (X_o)



2 NS/DIV
SHIFT $A_0 \rightarrow A_1$
(14-F) (3-A)

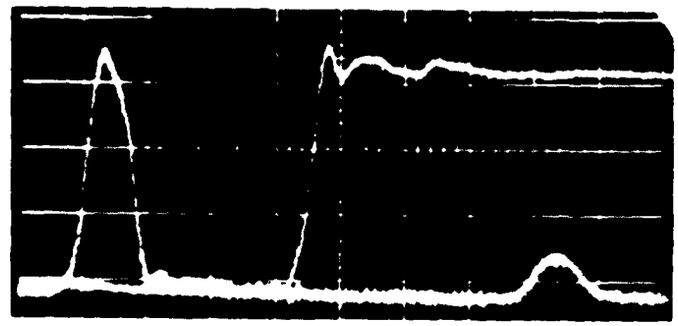


2 NS/DIV
SHIFT $A_1 \rightarrow A_2$
(14-F) (3-E)

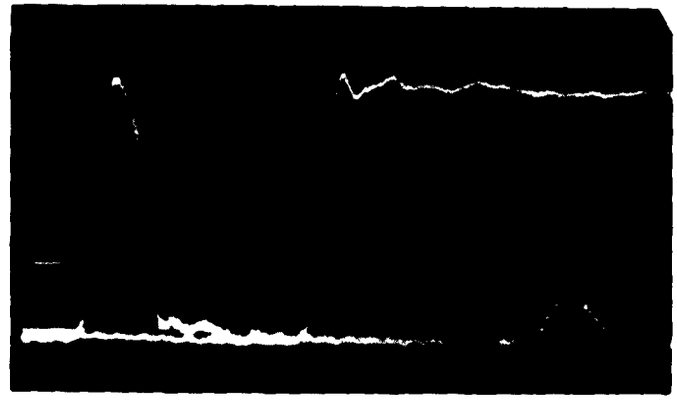


2 NS/DIV
SHIFT $A_2 \rightarrow A_3$
(14-F) (8-E)

Figure 2-3. Logic Transit Times (Sheet 1 of 7)



2 NS/DIV
SHIFT $A_3 \rightarrow A_0$
(14-F) (8-A)

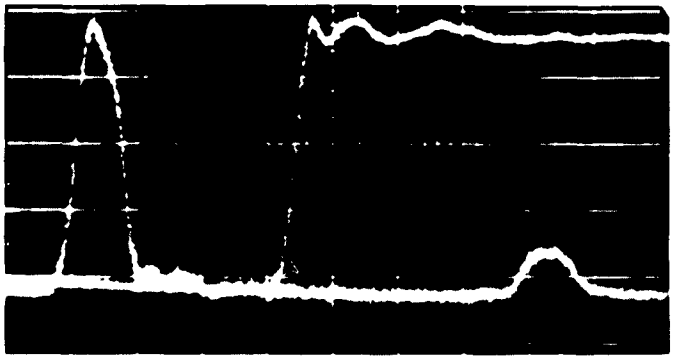


2 NS/DIV
TRANSFER $X_0 \rightarrow A_3$
(15-F) (8-E)

2 NS/DIV
TRANSFER $X_1 \rightarrow A_0$
(15-F) (8-A)

Figure 2-3. Logic Transit Times (Sheet 2 of 7)

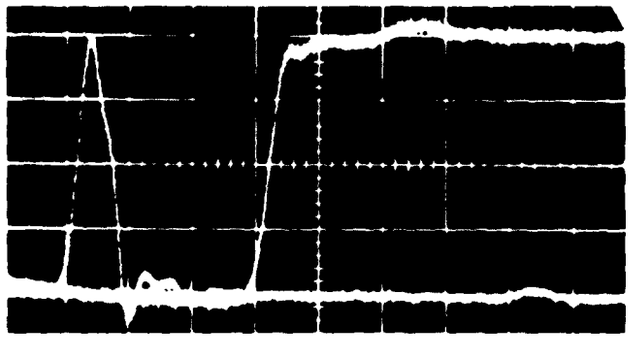
2 NS/DIV
TRANSFER $X_2 \rightarrow A_1$
(15-F) - (3-A)



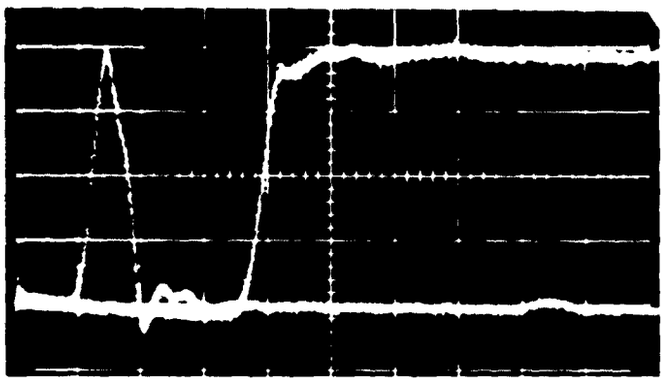
2 NS/DIV
TRANSFER $X_3 \rightarrow A$
(15-F)-(3-E)

2 NS/DIV
TRANSFER $A_0 \rightarrow X_0$
(12-F) (4-P)

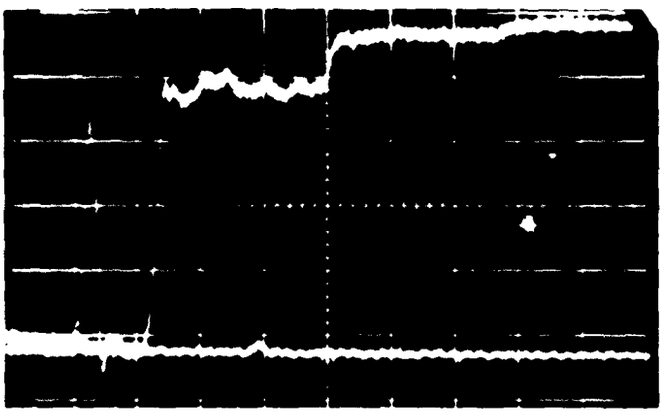
Figure 2-3. Logic Transit Times (Sheet 3 of 7)



2 NS/DIV
A → X_0 X_1 BIT
(12-F)(11-P)

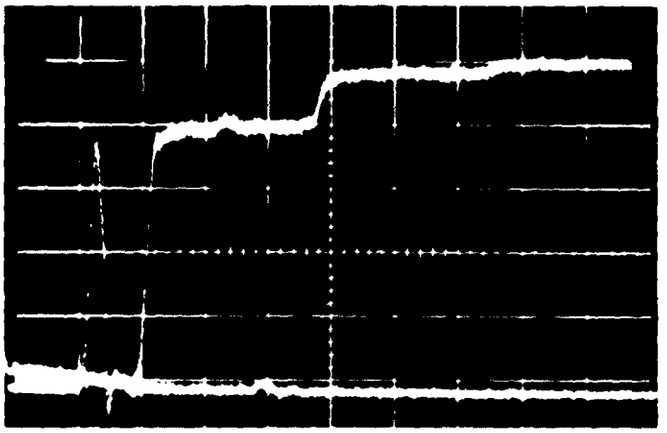


2 NS/DIV
TRANSFER A_2 → X_2
(12-F)(3-N)

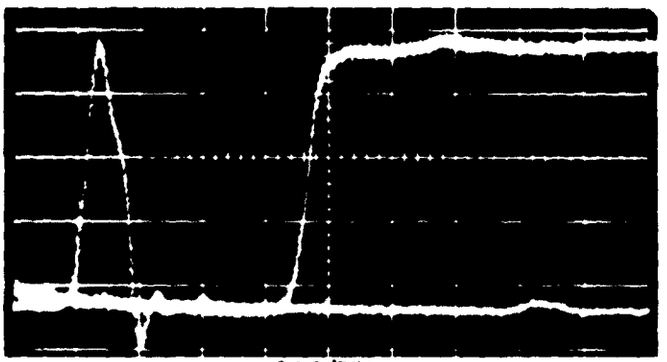


5 NS/DIV
TRANSFER A_3 → X_3
(12-F)(11-N)

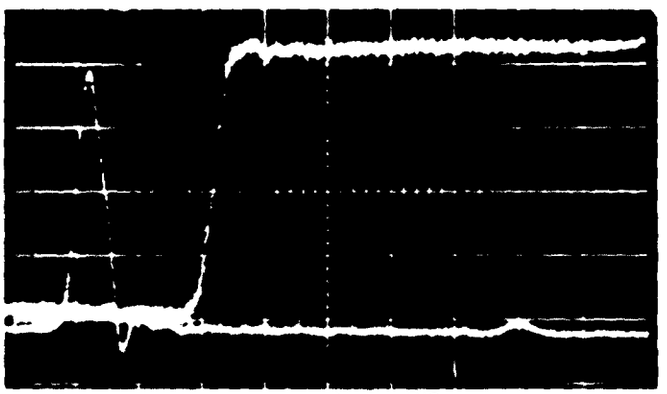
Figure 2-3. Logic Transit Times (Sheet 4 of 7)



5 NS/DIV
TRANSFER PARITY BIT FROM A → X
(12-F) → (11M)

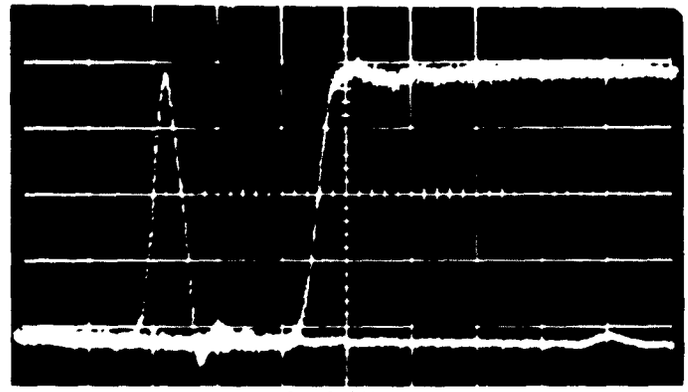


2 NS/DIV
DELAY BETWEEN C/PM(4-R) → PARITY BIT
IN 4-REG.(8-E)

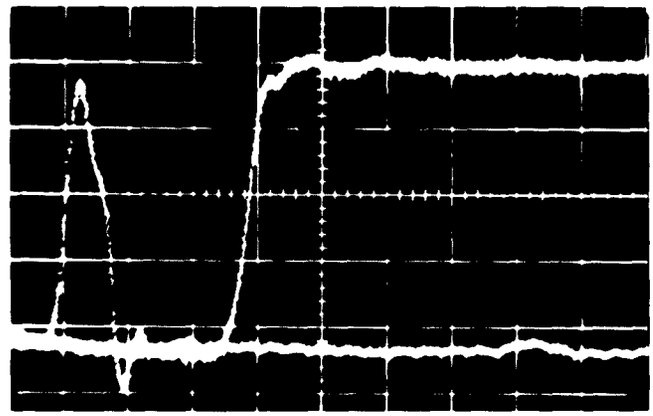


2 NS/DIV BIS.
CLPC 13-G TO 10-K 3 ϕ
(BEST CASE)

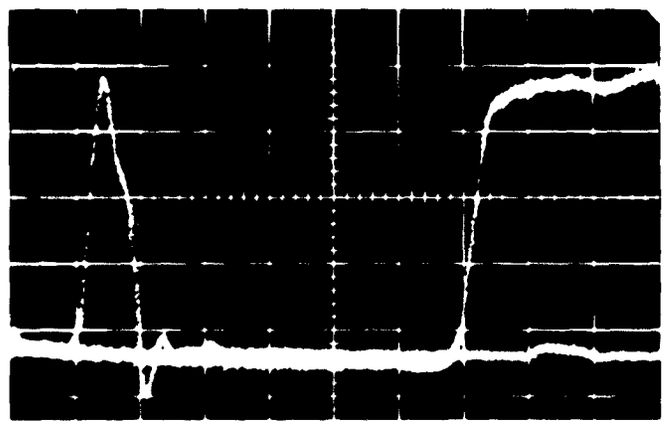
Figure 2-3. Logic Transit Times (Sheet 5 of 7)



2 NS/DIV BIS
CLPC 13-G TO 6V 1ϕ
(WORST CASE)



2 NS/DIV
COUNT 1ST BIT (X.)
(2-R) (4-P)



2 NS/DIV
COUNT 4TH BIT (X_3)
(2-R) (11-M)

Figure 2-3. Logic Transit Times (Sheet 6 of 7)

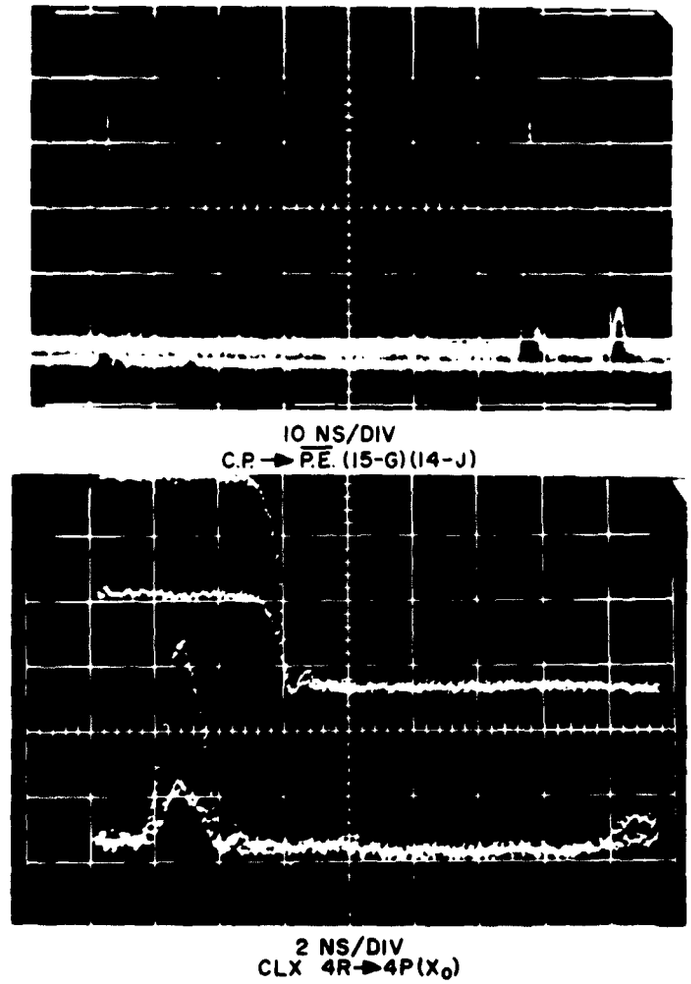


Figure 2-3. Logic Transit Times (Sheet 7 of 7)

B. A REGISTER TESTING

During this quarter, the accummulator register, or A register, the principal arithmetic unit of the Logic Subsystem was tested before being incorporated into the main frame. This register performs the functions of counting, shifting and transferring (Figure 2-5). It contains 10 bistable gates, 24 OR gates, 31 AND gates and 1 load wafer. The A register test frame is shown in Figure 2-6.

TABLE 2-4
DELAYS THROUGH PARITY CHECKER

Ref.	Level # and Wafer #	Reset Time for Bistables (NS)
15-G(C. P.)	1 6-V	9. 2
15-G(C. P.)	1 7-V	9. 4
3-V	2 10-K	3. 4
2-V	2 10-K	3. 4
3-V	3 7-J	5. 3
14-K	3 7-J	3. 3
3-K	4 4-J	3. 6
3-J	14 -J	1. 8
3-J	S 11-J	3. 4
1S-K	15-J	3. 0

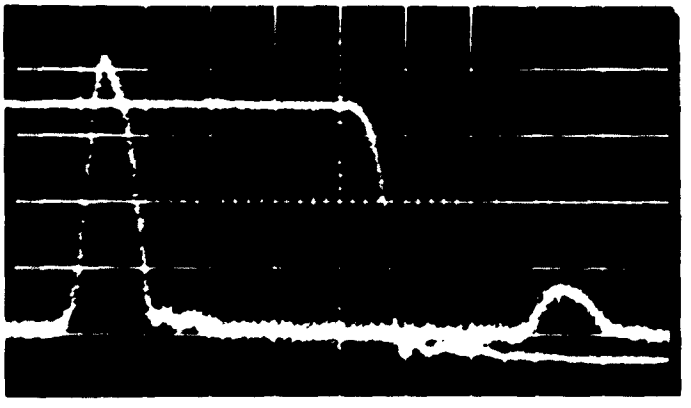
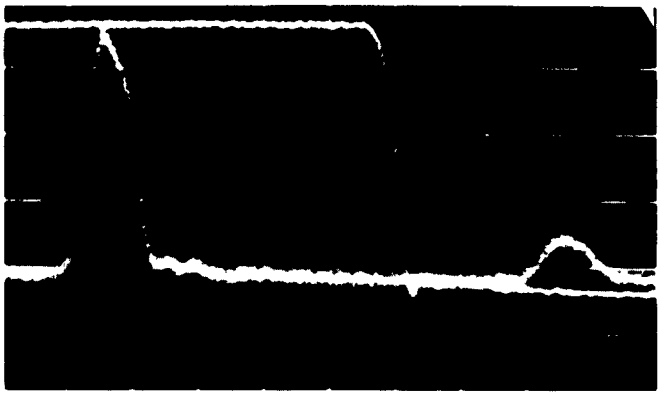
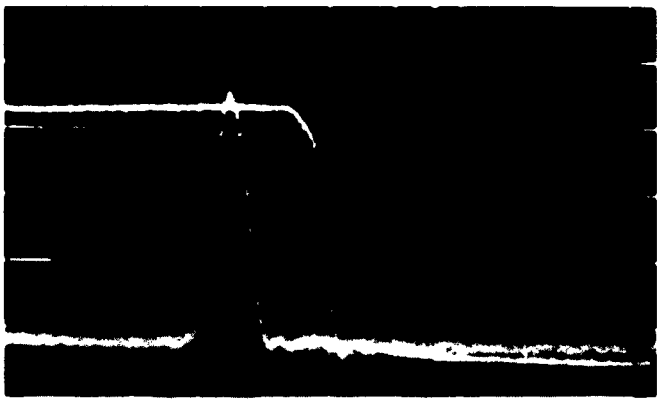


Figure 2-4. Parity Checker Delays (Sheet 1 of 4)



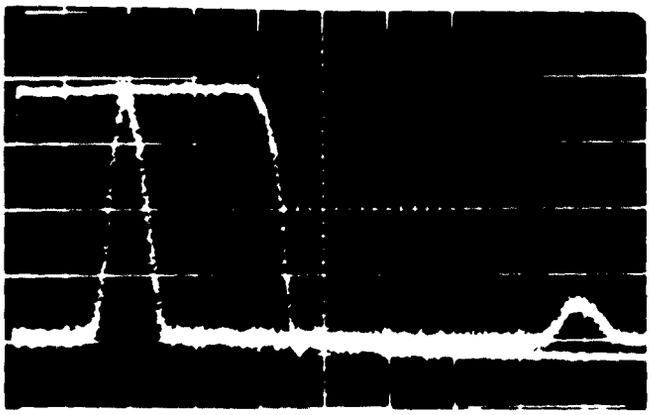
2 NS/DIV
15-G (C.P.) → 7-V (BIS 2)

2 NS/DIV
3-V → 10-K (3)

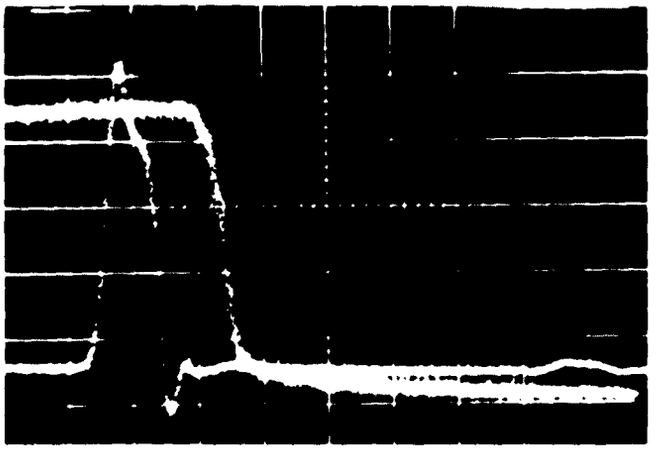


2 NS/DIV
2V → 10-K(3)

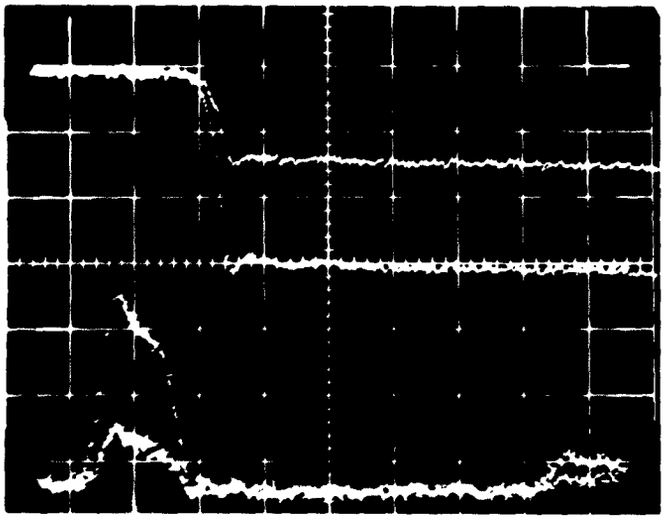
Figure 2-4. Parity Checker Delays (Sheet 2 of 4)



2 NS/DIV
3-V → 7-J(4⊕)

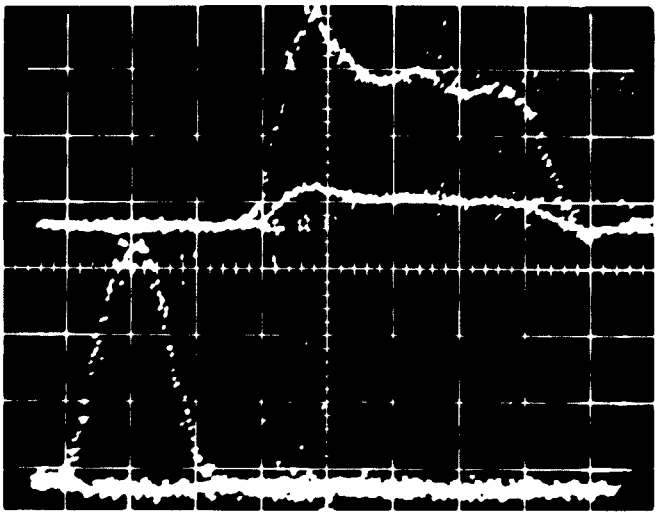


2 NS/DIV
14-K → 7-J(4⊕)

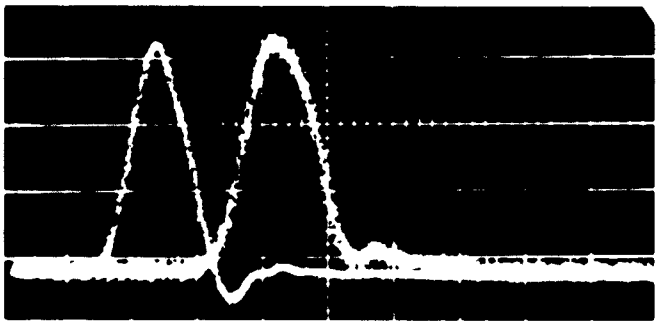


2 NS/DIV
3-K (DELAY) → 4-J (5⊕)

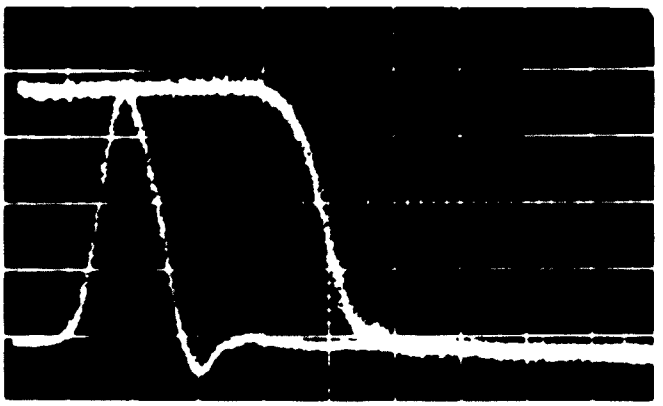
Figure 2-4. Parity Checker Delays (Sheet 3 of 4)



1NS/DIV 15-K → 15-5 (MdX3)



1 NS/DIV
3-J → 14-J ($\overline{PE}$)



1 NS/DIV
3-J → 11-J (6 ◆)

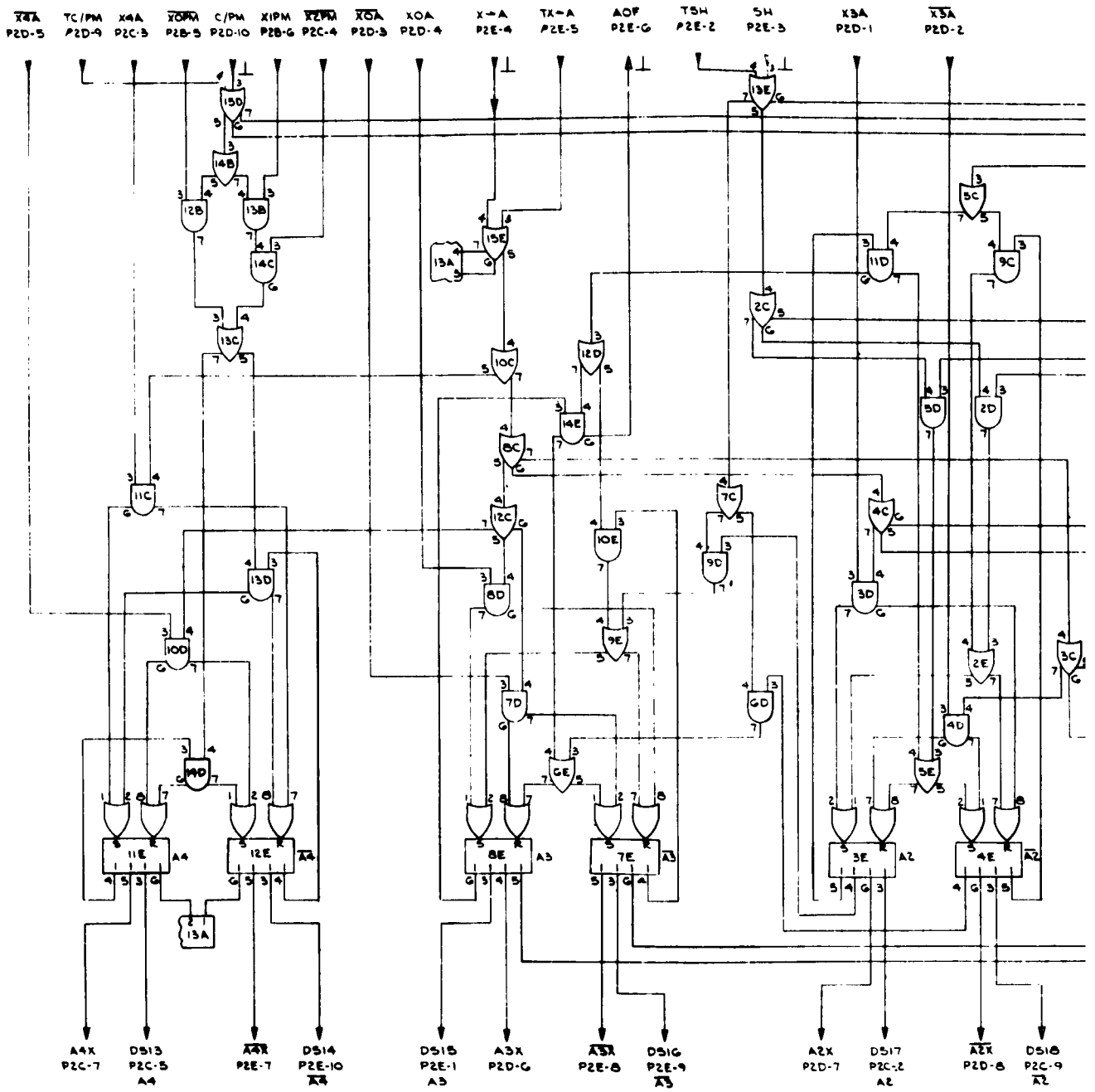
Figure 2-4. Parity Checker Delays (Sheet 4 of 4)

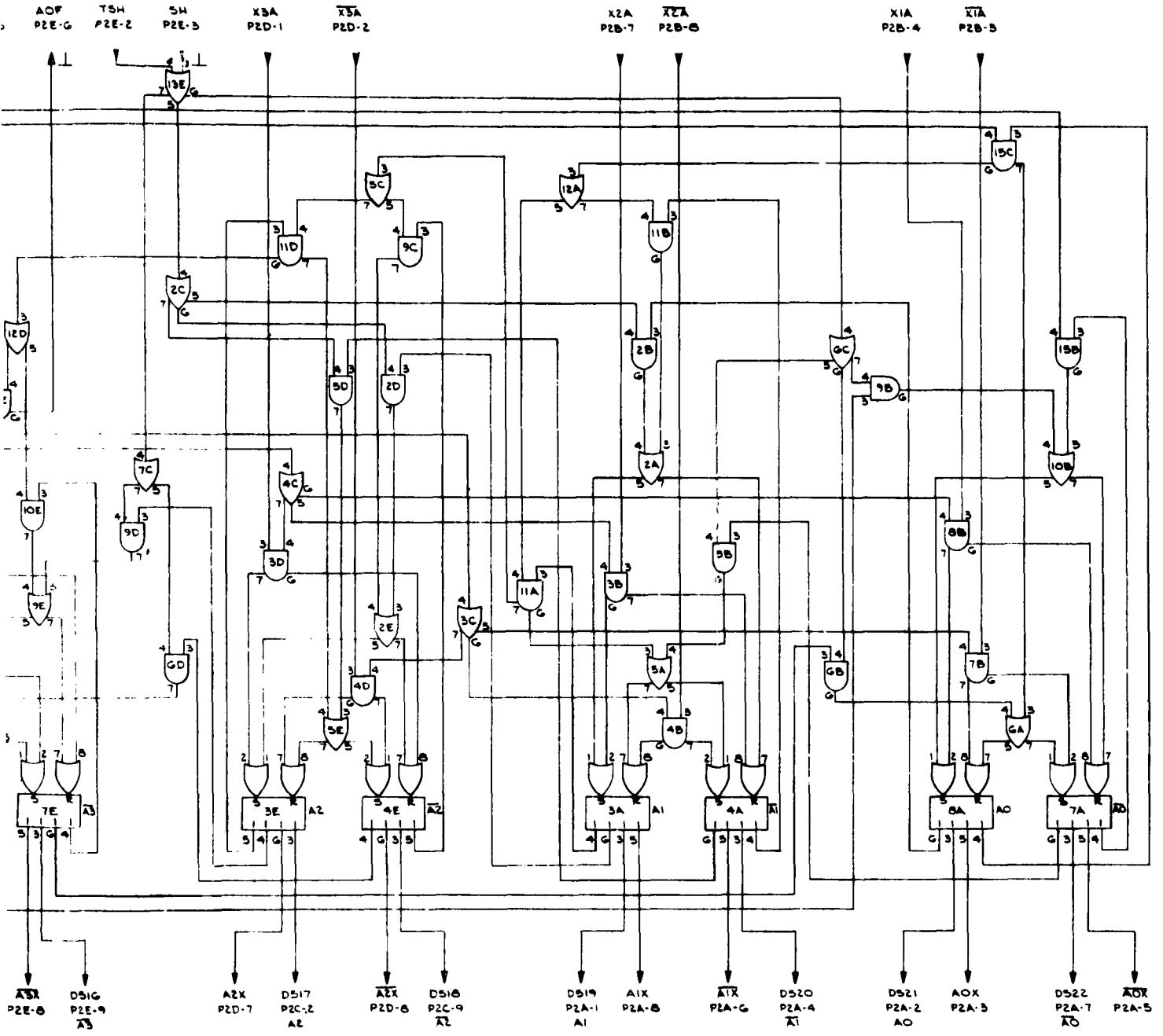
TABLE 2-5
COMPARISON OF LOGIC SUBSYSTEM OPERATION TIMES

Operation	Best Case (NS)	Actual Measured Time (NS)	Worst Case (NS)
Clear X	2.5	3.6	8.5
C.P. $\overline{PE}$	62.7	65	79.1
Clear PC	3.4	5.1	8.9
X⟶A	5.1	7.6	14.1
SHIFT	6.0	7.4	12.5
Count & PM	5.2	6—12 (4th Bit Count)	22.6
A⟶X	3.8	6	12.1

TABLE 2-6
COMPARISON OF LOGIC SUBSYSTEM CONTROL UNIT OUTPUTS

Control Unit Outputs	Earliest Time (NS)	Actual Measured Time (NS)	Latest Time (NS)
X⟶A	0	-	-
SHIFT	14.5	15	18.3
C/PM	27.8	29	36.4
A⟶X	51.7	54.2	66.1
C P_2	62.2	66.6	79.3
$\overline{PE2}$	0	-	-
CL_2PC	5.7	5.0	9.2
X⟶A	10.5	9.4	16.6


X4A P2D-5
TC/PM P2D-9
X4A P2C-3
XOPM P2B-5
C/PM P2D-10
XIPM P2B-6
XEPM P2C-4
XOA P2D-3
XOA P2D-4
X→A P2E-4
TX→A P2E-5
AOF P2E-6
TSH P2E-2
SH P2E-3
X3A P2D-1
X3A P2D-2
A4X P2C-7
DS13 P2C-5 A4
A4R P2E-7
DS14 P2E-10 A4
DS15 P2E-1 A3
A3X P2D-6
A3R P2E-8
DS16 P2E-9 A3
A2X P2D-7
DS17 P2C-2 A2
A2R P2D-8
DS18 P2C-9 A2



NOTES
1 FOR TRUTH TABLE AND LEGEND OF LOGIC SYMBOLS SEE PNA-G-28
2 UNLESS OTHERWISE DESIGNATED ALL INPUTS AND OUTPUTS ARE LEVELS.

Figure 2-5. A-Register Logic Diagram

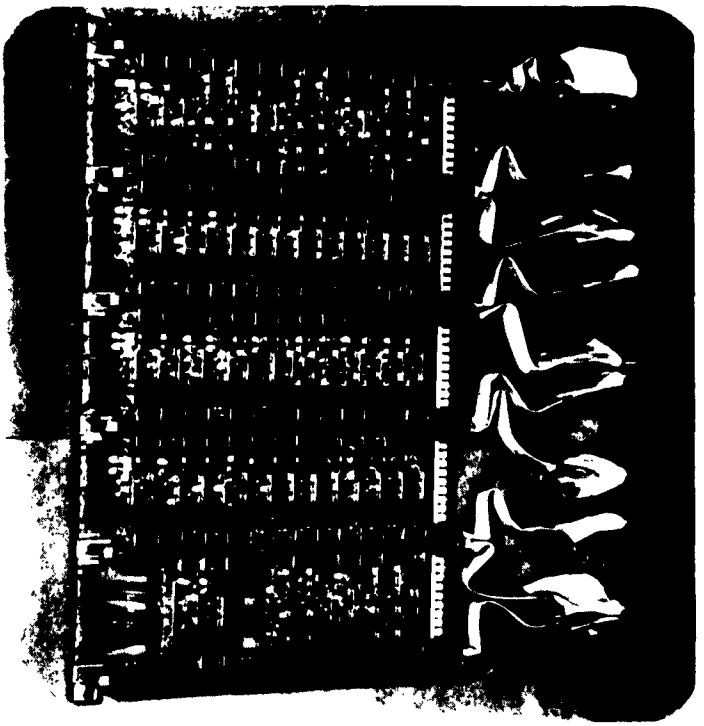


Figure 2-6. A-Register Test Frame

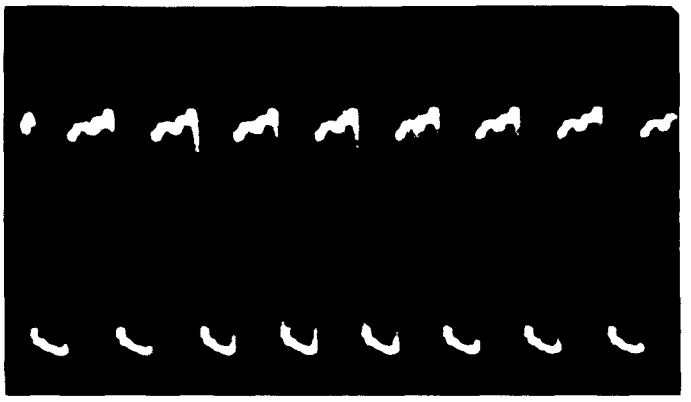
The first obstacle encountered was faulty power supply connections. After correcting this condition, the biases were applied and obvious discrepancies in d-c operating characteristics were corrected. The chief cause of erroneous d-c operation was poor solder connections.

Next a-c operation was tested by going through the various functions the A register must perform using 60 cycle pulses. Here too, poor solder connections and a few out-of-specification components were found to be hindering proper operation. Once these defects were corrected, the operating biases were checked for acceptable tolerance limits and found to be slightly deficient. This problem was solved by replacing the remaining out-of-specification components within specification units.

In raising the a-c operating frequency into the megacycle range, a few more problems were encountered; mainly the existence of an abnormally large transient voltage on the 90-mv d-c power supply lines. This problem was alleviated by terminating the d-c power lines. Final operation consisted of shifting and counting at 135 mc, and proper transfers (Figure 2-7).

C. LOGIC SUBSYSTEM FABRICATION

The entire Logic Subsystem was completed and is now operational. The seven logic frames were all inserted into the main frame and wired together. The console was completed and added to the system.

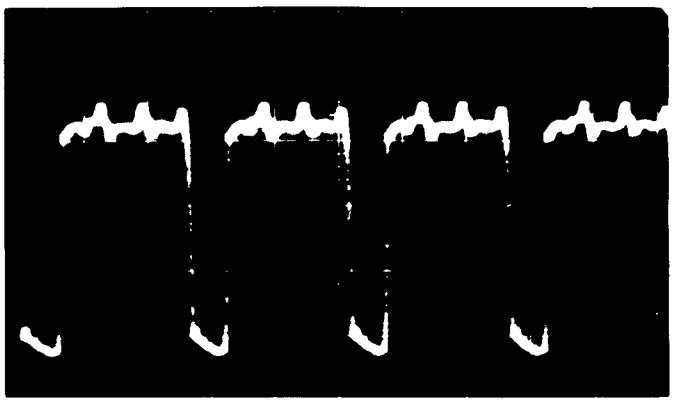


20 NS/DIV
(A) 1010 PATTERN

20 NS/DIV
(B) 1100 PATTERN

20 NS/DIV
(C) 1000 PATTERN

Figure 2-7. 135-mc Shift Patterns in A Register (Sheet 1 of 2)



20 NS/DIV
(D) 1110 PATTERN

Figure 2-7. 135-mc Shift Patterns in A Register (Sheet 2 of 2)

A shielding box has been added to the main frame to shield it from external noise. This box completely encloses the frames with metal walls and metal screening.

Cooling the subsystem became a problem due to varying room temperature. Since this causes unreliable operation, an air-conditioner was positioned under the cooling fans so that it is now possible to maintain a stable ambient temperature.

D. MAIN CONSOLE CHECKOUT

The main console, Figure 2-8, has been completed and checked out, and is presently being used with the main frame. The console was successfully checked by testing all lamps, driving them from a bistable circuit and testing all AND inputs for proper magnitude (i. e. sufficient amplitude to perform the AND function but not enough to exceed the threshold current). The console schematic is shown in Figure 2-9.

The only malfunction caused by the console was due to a logic error in which the subsystem operation was dependent upon the actions of both sides of a dpdt switch. This mistiming, which caused faulty operation in some modes, was corrected.

Crosstalk is eliminated by the use of coaxial table for all signal lines to the console as well as all interconnections within the console. In addition current sources with long time constants were used rather than voltage sources to prevent overshoot of AND gate levels. These precautions have led to the present satisfactory operation.

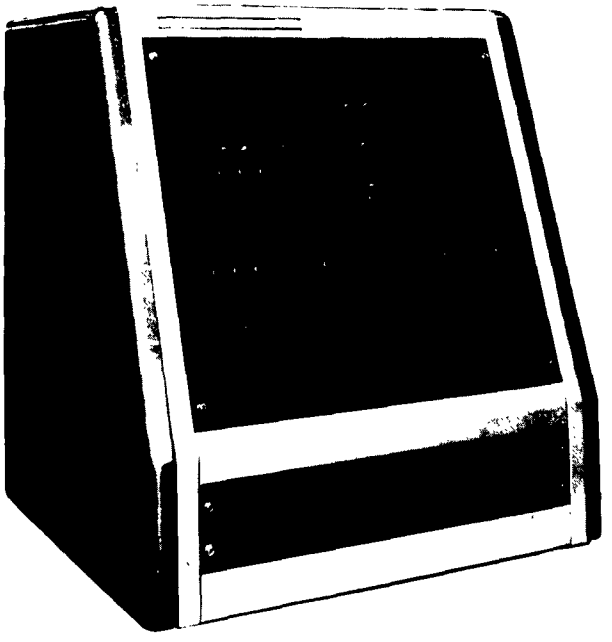


Figure 2-8. Logic Subsystem Console

E. WAFER FABRICATION

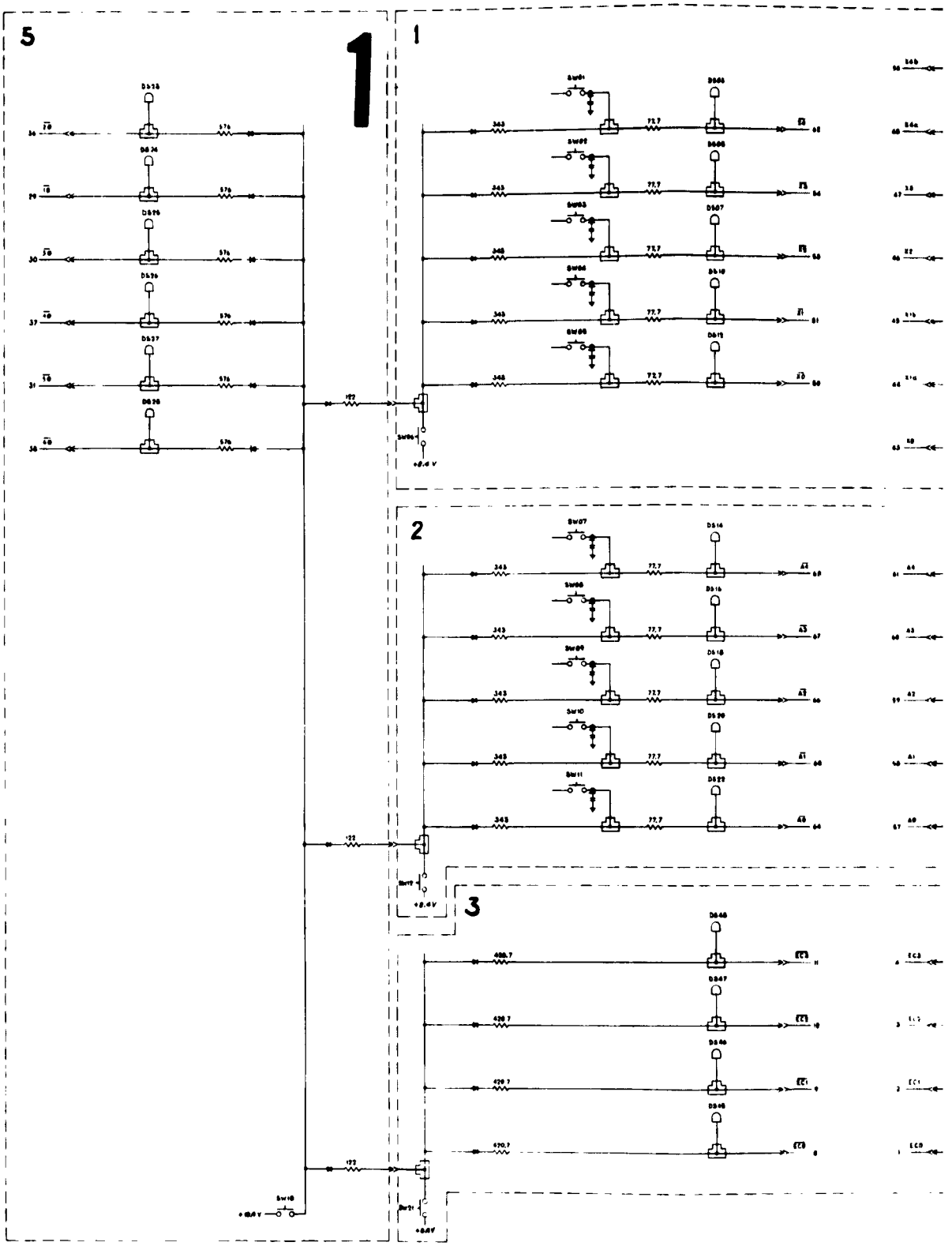
All wafers were completed for the Logic Subsystem and memory peripheral equipment. The fabricating was done using 50% soldering and 50% welding techniques. Final results indicate poor connections of diodes in both the welded and soldered wafers. It is felt that some cold-solder connections were formed due to the short time cycle in the welding and soldering operation necessary because of the fragile devices.

Mounting losses have been reduced to a minimum with the soldering technique and therefore all future wafers will be soldered. Several spare wafers are presently being fabricated for use if needed.

1. New Wafer Construction

A new wafer package in which all components are inserted into the circuit mechanically was investigaed. This package uses no solder. Contacts are made by sandwiching all components between two printed circuit boards and locking the package together.

Figure 2-10 illustrates a typical wafer. The circuit to be fabricated is laid out onto two printed circuit boards such that when transversing a component, the path leads from board #1 to board #2, or vice-versa. The two boards are backed with a heavy ground plane for mechanical support.


5
1
1
2
3

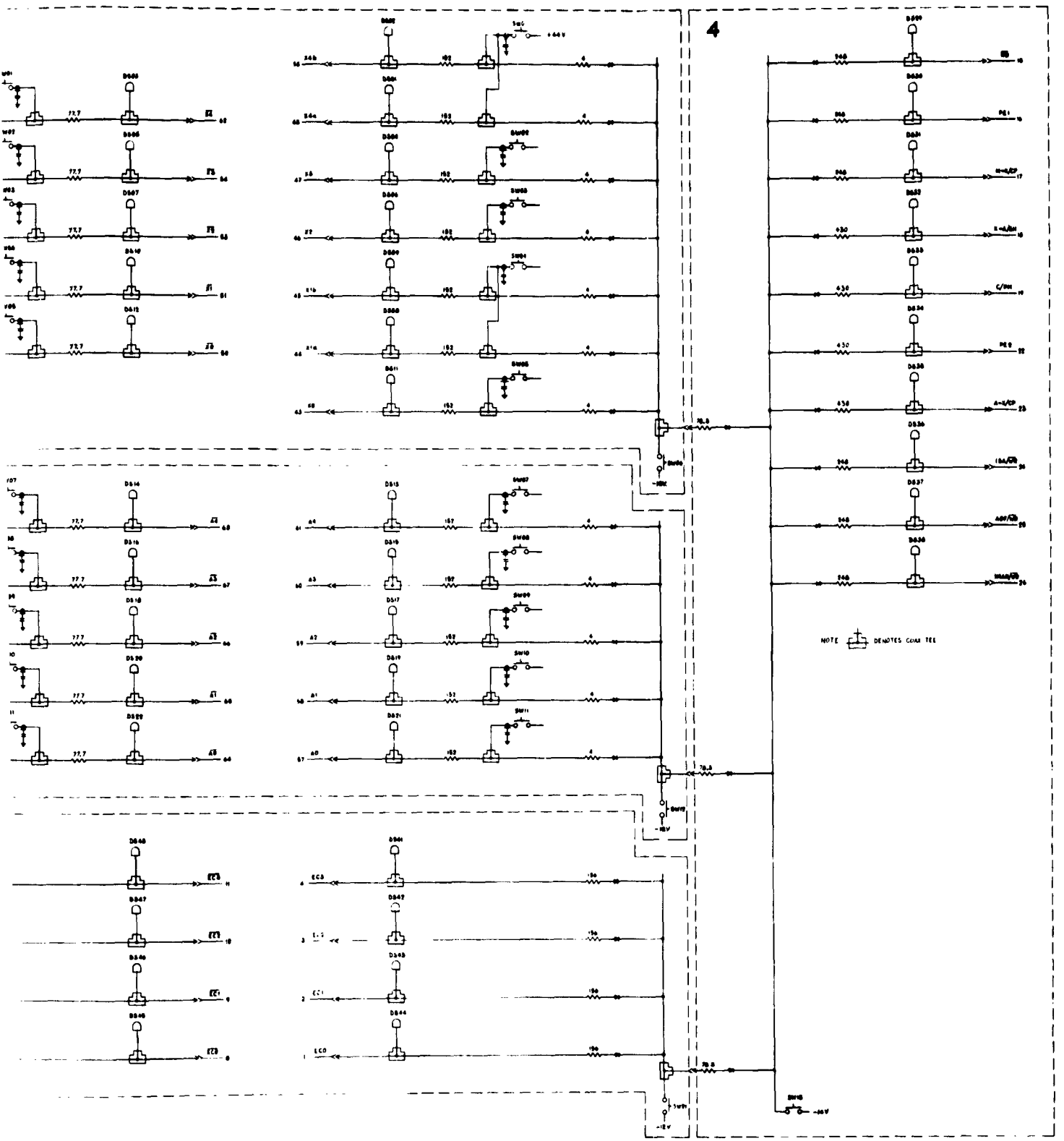
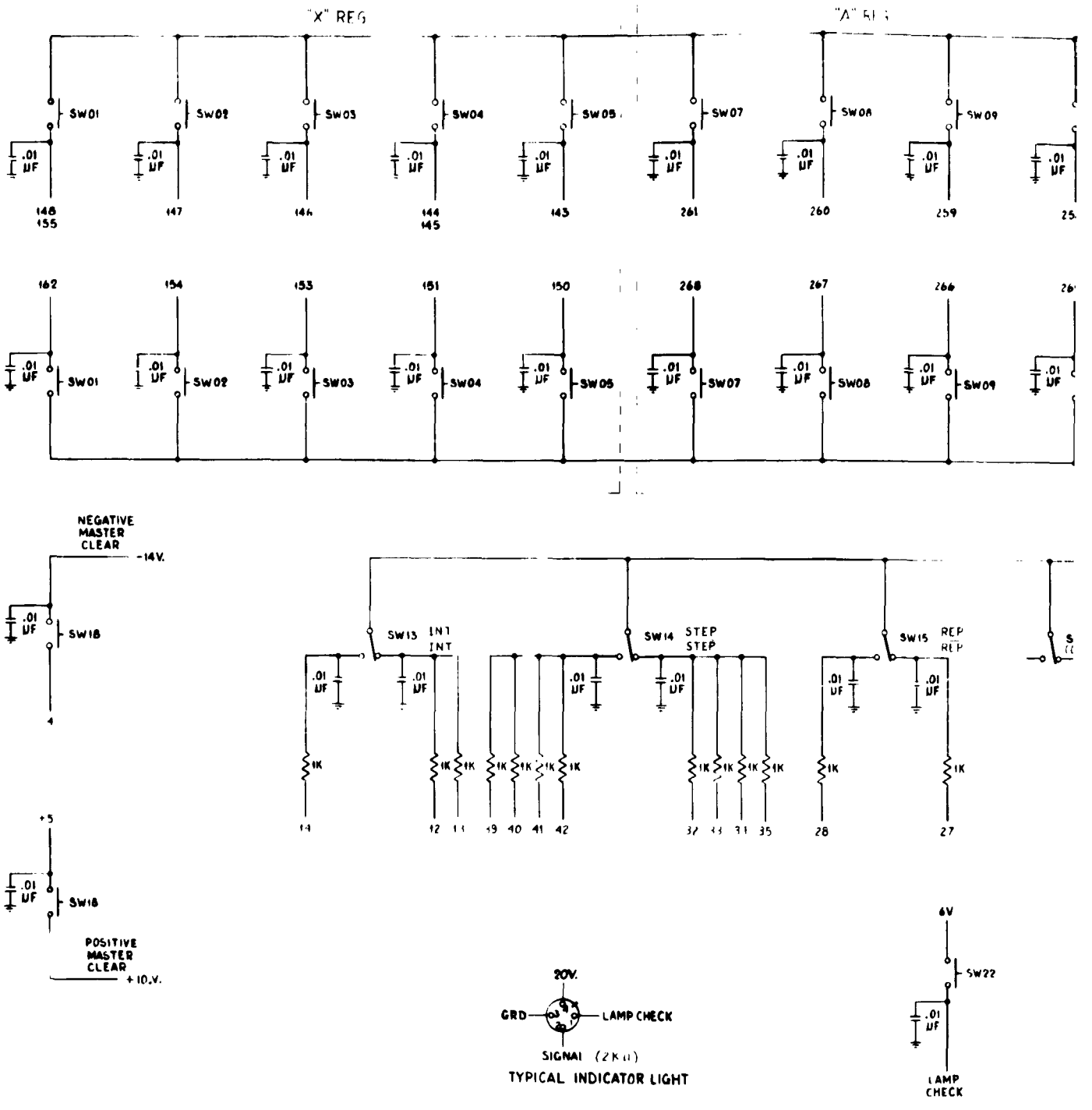


Figure 2-9. Logic Subsystem Console
(a) Reset Control


"X" REG
"A" REG
SW01
SW02
SW03
SW04
SW05
SW07
SW08
SW09
.01 MF
148
155
147
144
145
143
261
260
259
162
154
153
151
150
268
267
266
NEGATIVE MASTER CLEAR
-14V.
SW18
4
+5
POSITIVE MASTER CLEAR
+10.V.
SW13 INT
INT
SW14 STEP
STEP
SW15 REP
REP
1K
14
12
49
40
41
42
37
28
27
20V.
GRD
LAMP CHECK
SIGNAL (2K Ω)
TYPICAL INDICATOR LIGHT
6V
SW22
LAMP CHECK

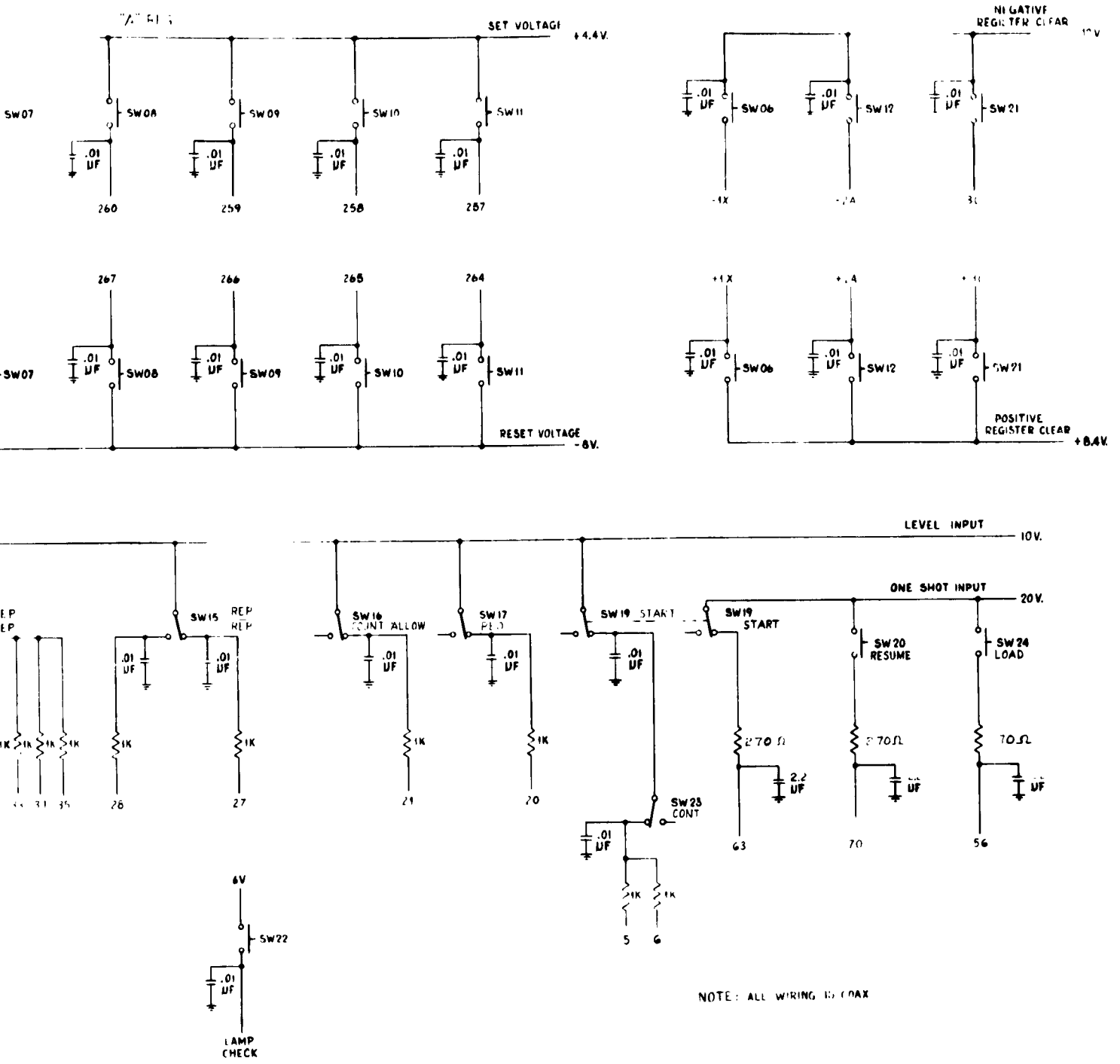


Figure 2-9. Logic Subsystem Console (b) Indicator Control

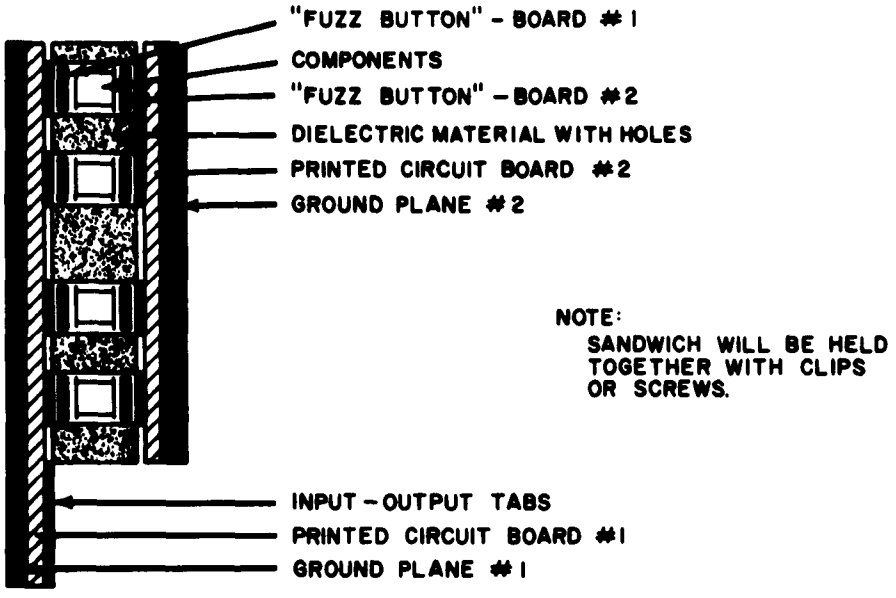


Figure 2-10. Sandwich Wafer Section

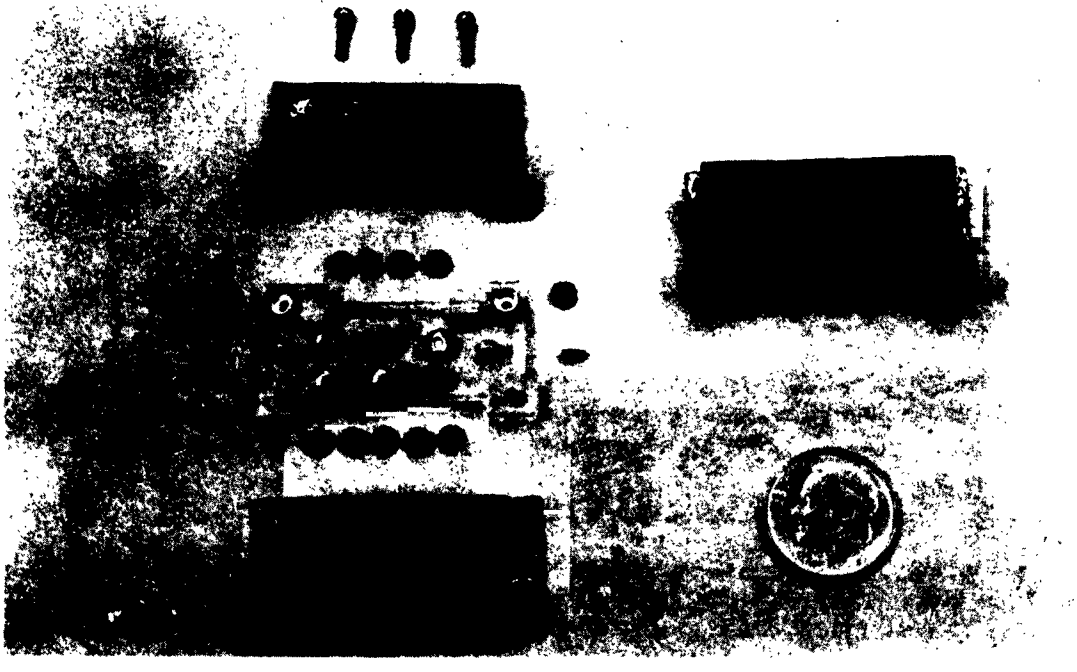


Figure 2-10a. Sandwich Wafer (assembled & disassembled)

Contacts between components and the printed boards are made by gold "fuzz buttons". The "fuzz button" is a fine gold wire mesh formed into a pellet, the number of wires used in the pellet varies the resiliency of the "fuzz button". A good spring contact is made when fewer wires are used.

A typical wafer is assembled as follows:

a) Printed circuit board #1 with its ground plane is laid flat with circuit facing up. (It should be noted here that high-K capacitors may be placed onto the printed circuit board at any location. Also, any point in the circuit that has a grounded component has the circuit board removed from that position to the ground plane).

b) A dielectric plane with holes properly located to reveal the parts of the parts of the circuit to which components are to make contact is placed on top of board #1.

c) A "fuzz button" is placed into each hole in the dielectric.

d) Components (tunneling devices with no tabs and end-capped resistors) are dropped onto the "fuzz button".

e) A second set of "fuzz buttons" is now placed over all components.

f) Printed circuit board #2 is then positioned over the entire structure and the sandwich is clamped together with locking clips or screws.

g) Input-output points are made available by extending one printed circuit board beyond the other.

Several advantages are available in this construction, such as, easy assembly, easy component replacement, good shielding to adjacent wafers, and more compact packaging.

The first attempt to package a circuit using this technique was made on a standard OR curcuit (Figure 2-10a).

Initial results indicate good contact being made on all parts. The wafer was operated at 200 megacycles as shown in Figure 2-11. The next attempt will be to build a bistable and AND wafer to compare them with standard fabrication.

F. CHECKOUT OF MEMORY ADDRESS DECODER

An all tunnel diode, 32-word memory address decoder has been fabricated, checked out electrically and integrated with other memory peripheral circuitry. It consists of 22 AND gates, 8 OR gates, 12 bistables, 7 pulse amplifiers and 1 one-shot.

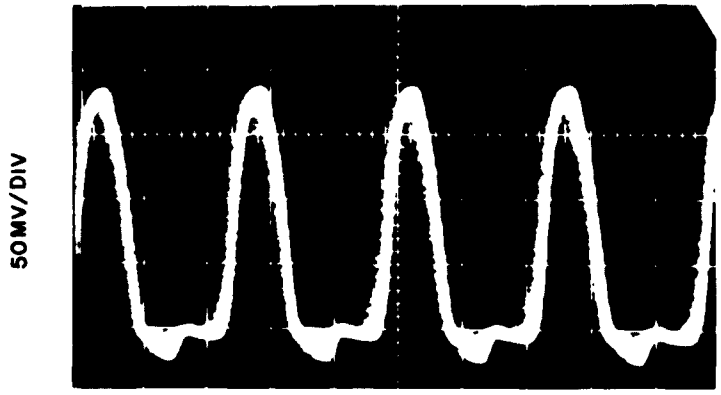


Figure 2-11. Output of Sandwich Wafer

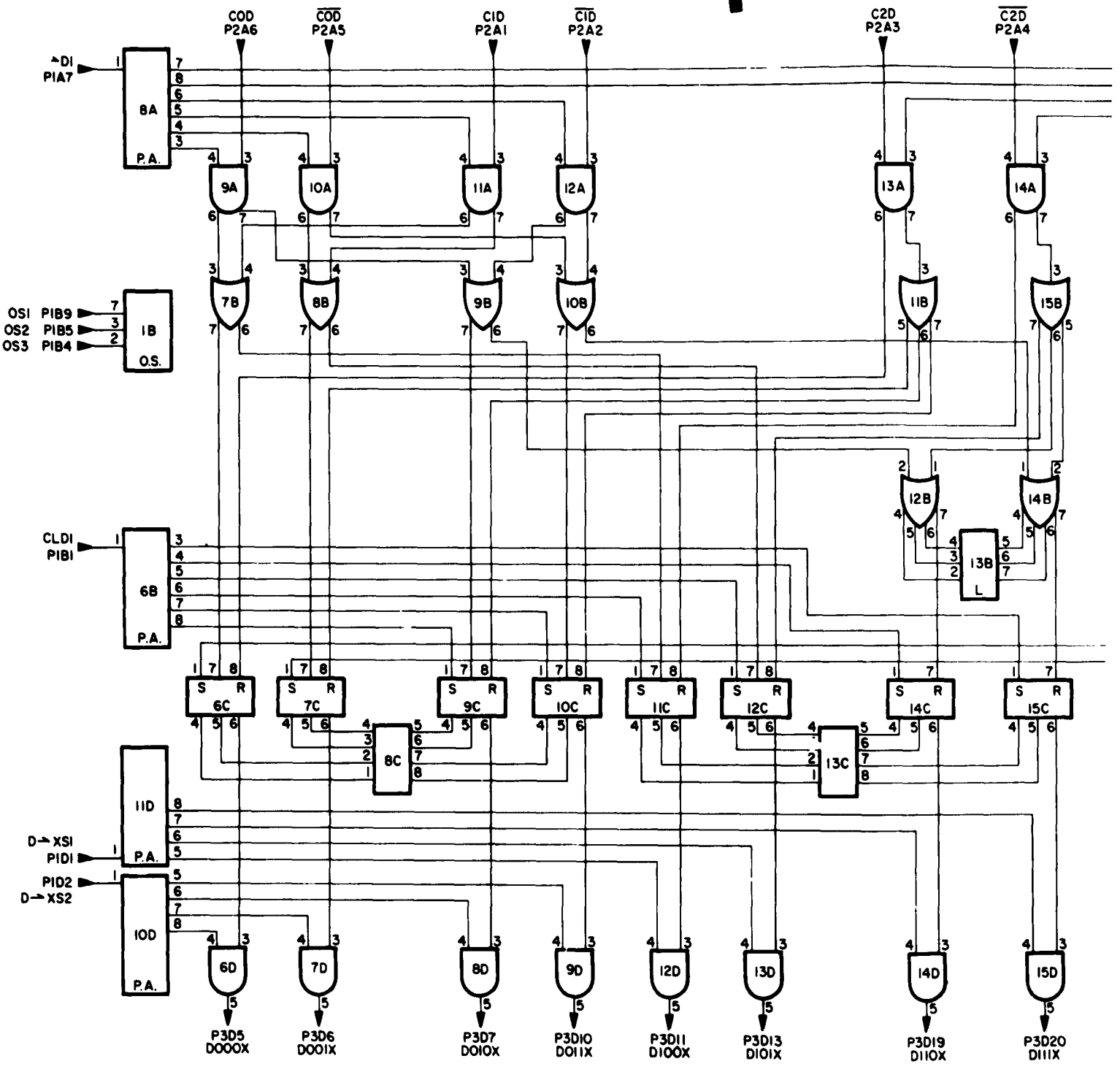
The following procedure was employed in its checkout:

Each wafer was initially tested with worst-case signal inputs and voltage biases. The wafers were then inserted into a frame and the system was debugged at a low (120 cps) repetition rate. After this phase was completed, the system repetition rate was increased to approximately 30 megacycles where reliable operation was realized. The final phase of the checkout consisted of integrating the decoder with other memory peripheral circuitry, namely the memory address counter and the X-Y memory switches. All three of these above units are now operating reliably at full speed in conjunction with one another. Also the decoder continued to run reliably within the following voltage ranges:

+90 mv supply	70 mv — 101 mv	with +6 and -6 volt supplies at nominal values
+6.0 v supply	5.84 v — 6.20 v	with -6 volt and +90 mv supplies at nominal values
-6.0 v supply	-5.45 v — 6.40 v	with +6 volt and +90 mv supplies at nominal values.

Figure 2-12 is a logical layout of the decoder. A detailed description of the logical function of the memory address counter-decoder-X & Y switch system was explained in IRR-13 Chapter 4, and therefore at this juncture will be omitted.

Figure 2-13 shows the timing scheme used for the decoder.


1
COD P2A6
COD P2A5
CID P2A1
CID P2A2
C2D P2A3
C2D P2A4
DI PIA7
8A P.A.
9A
10A
11A
12A
13A
14A
OSI PIB9
OS2 PIB5
OS3 PIB4
1B O.S.
7B
8B
9B
10B
11B
15B
12B
14B
13B L
CLDI PIBI
6B P.A.
6C
7C
9C
10C
11C
12C
14C
15C
8C
13C
11D P.A.
D→XSI PIDI
PID2 D→XS2
10D P.A.
6D
7D
8D
9D
12D
13D
14D
15D
P3D5 D000X
P3D6 D001X
P3D7 D010X
P3D10 D011X
P3D11 D100X
P3D13 D101X
P3D19 D110X
P3D20 D111X

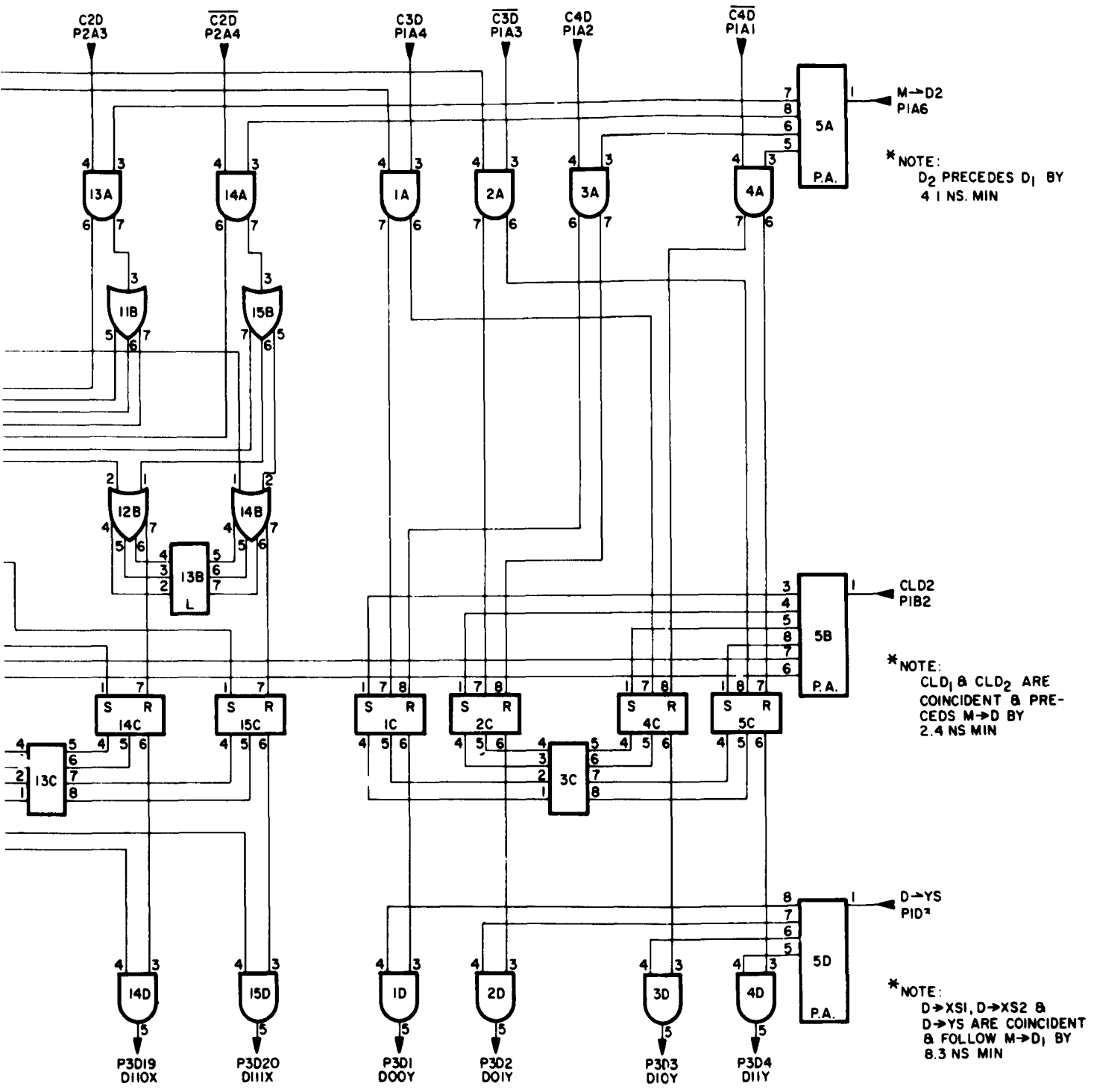


Figure 2-12. Memory Address Decoder Logic Diagram

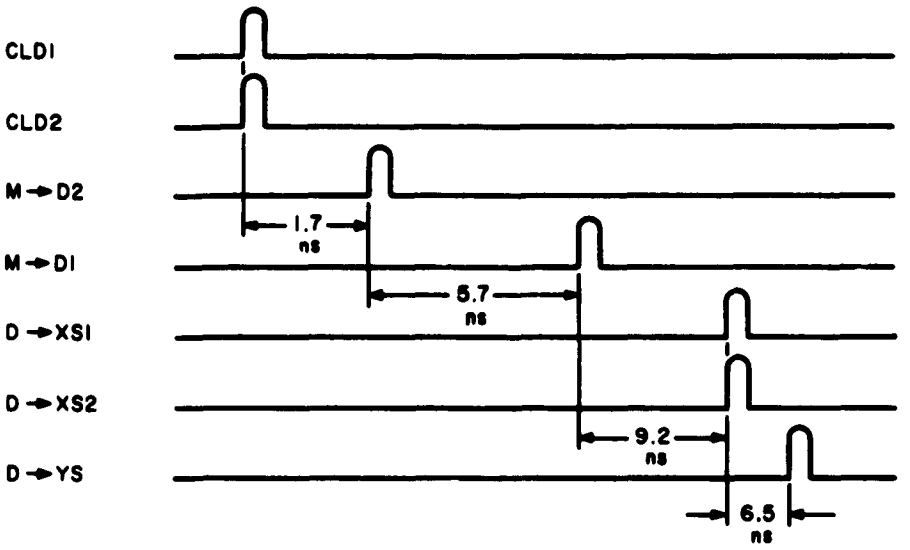


Figure 2-13. Timing Scheme For Memory Address Decoder

Some delay measurements were made as shown in Figure 2-14. From this photograph it can be seen that the worst-case delay, i. e., the longest path in the decoding process is approximately 5. 6 nanoseconds. This photograph shows the elapsed time between when the input AND gate (8A) fires and when bistable (15c) is reset.

The X and Y outputs from the decoder are shown in Figure 2-15.

Figure 2-16 shows the completely integrated memory address counter-decoder-X and Y system.

It should be noted that the plugable wafer connectors described in IRR-13A are being employed throughout both the memory address decoder and counter units. The ease of wafer removal afforded by this connector greatly facilitates debugging of these units. Some erratic wafer behavior was introduced by these connectors, but for the most part, this has been reduced to a tolerable minimum.

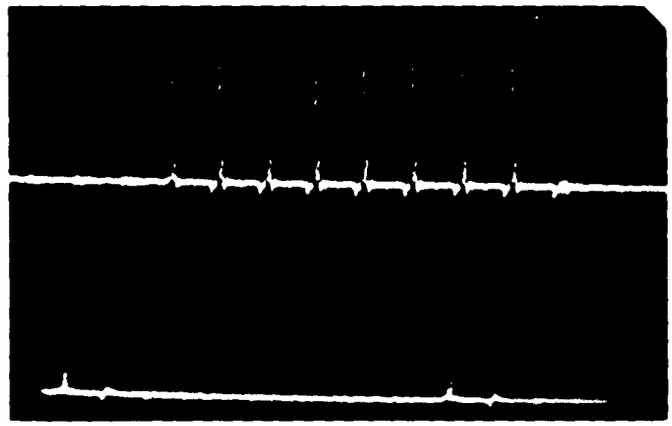
G. COMBINING THE LOGIC AND MEMORY SUBSYSTEMS

In order to combine the Logic Subsystem with the Memory Subsystem, two logic components (read-write register and inhibit sense amplifier driver) are necessary. The read and write registers provide electrical compatibility while the inhibit sense amplifier driver is necessary to write information from the logic X register into the memory.

The read and write register is now in the process of being debugged and the wafers on the inhibit sense amplifier driver are now being worst-case tested.

2 NS/DIV

Figure 2-14. Decoder Delays



Y + X OUTPUTS FROM DECODER

Figure 2-15. X and Y Outputs from the Decoder

H. SYSTEM IMPROVEMENT STUDIES

1. Protection From Current Source to Bias Voltage Shorts

The logic circuits comprising the memory peripheral system are powered by laboratory bench-type power supplies. The +90 mv and -90 mv bias voltages are delivered by Trygons[1] and the -6 v and +6 v current sources are delivered by Power Design[2] Units. The distribution scheme is the same as that of the Logic Subsystem

[1] Power Supply type P20-2, Trygon Electronics Inc.
[2] Power Supply type 1210 Power Designs, Inc.

Figure 2-16. (a) Memory Address Counter and Decoder

Figure 2-16. (b) X-Y Switch Matrix

with all power lines in close proximity. This created a need for providing a special protection scheme to save the circuits from complete damage in cases of accidental current source voltage to bias voltage short circuits. Such a scheme was devised and incorporated into the Power Design power supplies. The scheme is essentially the same as that used in the Logic Subsystem power supply. Figure 2-17 through 2-20 show the schematic diagrams of the system.

Basically, the system works by rapidly short circuiting the power at both the input and the output ends of the regulator by means of silicon-controlled rectifiers. The short circuit current will open up a rapid acting magnetic circuit breaker as a final step in removing power from the load. A transistor switch is used to sense the overvoltage condition on the bias lines and to turn on the silicon-controlled rectifier (SCR). A 150-ohm resistor is used to discharge the 30,000 uf capacitor at the input end of the regulator after the circuit breaker has opened. Without this resistance, resetting the circuit breaker after a fault becomes very troublesome. The discharge R-C time constant is 4.5 seconds and hence the resetting of the circuit breaker should not be attemped until this length of time has elapsed. A 0.5-ohm resistor is used in series with TCR 501, to limit the short circuit current through that SCR.

Tests were made on the system by shorting the +90mv to +6v across a series combination of a tunnel diode and a clamp diode. The short was repeated 10 times and the diodes were not damaged. Another test, shown in Figure 2-21, was conducted to determine the shutting off waveforms. A solenoid operated mercury relay was used to create the fault condition. A Tektromix 585 oscilloscope was used in the single-sweep mode to observe and photograph the waveforms. It was found that the voltage at the +90mv point rose to 2v and fell down to approximately 500 mv within 0.5 us after a +6v overvoltage was applied. This was probably due to the effect of the inductance between the power supplies as it is too fast to be attributed to SCR action.

2. Low-Impedance Line Noise Tests

While the A register was being tested on the test frame, difficulty was experienced when high repetition rate shifting was attempted. The trouble was traced to the regulation on the +90-mv line. Probing on the wafer capacitances and along the distribution lines showed large peak-to-peak amplitude distrubances. These large disturbances were confined mainly to the column which housed the bistable wafers. Disturbance amplitude was found to be larger on the reset side of the wafers than on the set side. A decision to terminate these lines was made to get the system working. It was found that terminating only one line made the system work properly. Since this type of trouble did not show up before, it required considerable investigation which could not be carried out on the test frame. Thus it was decided to build a separate column of bistable wafers which could be set and reset at various repetition rates so that the disturbances on the distribution system could be studied. Such a column was built and run at 3 speeds - SKL; 50 mc; and 100 mc. First only one wafer was operated, and later another was added. The first wafer employed plug-in type construction while the second one was soldered as in the Logic Subsystem. This provided an opportunity to compare the two types of construction. It is planned to add two more bistable wafers and also to test OR wafers before this set of tests is concluded.

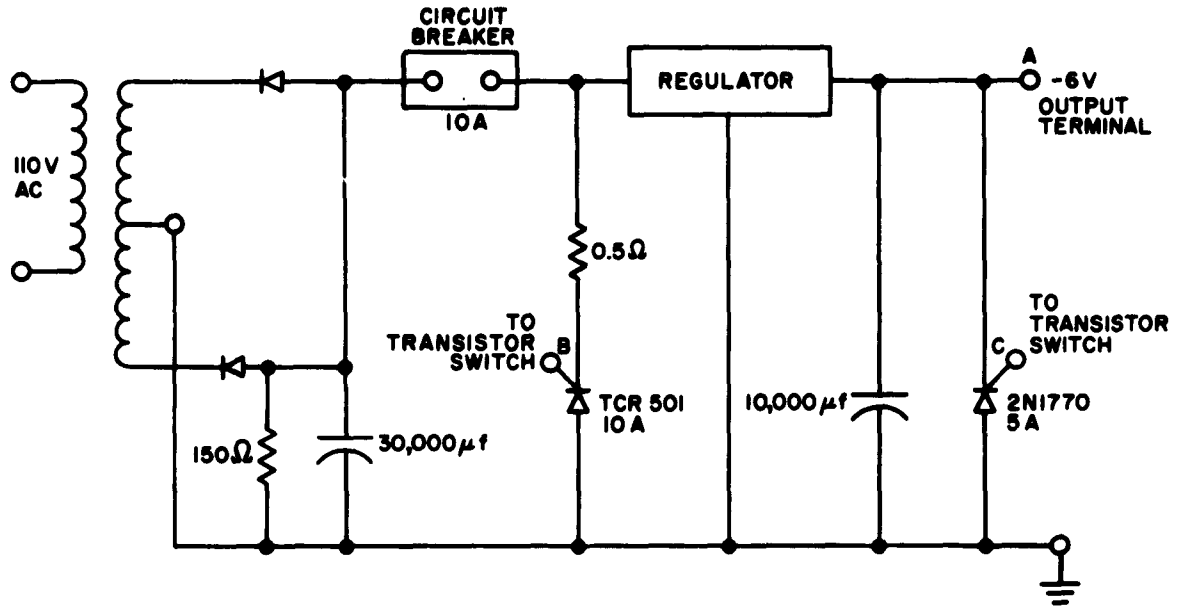


Figure 2-17. Protection Scheme for —6v Supply

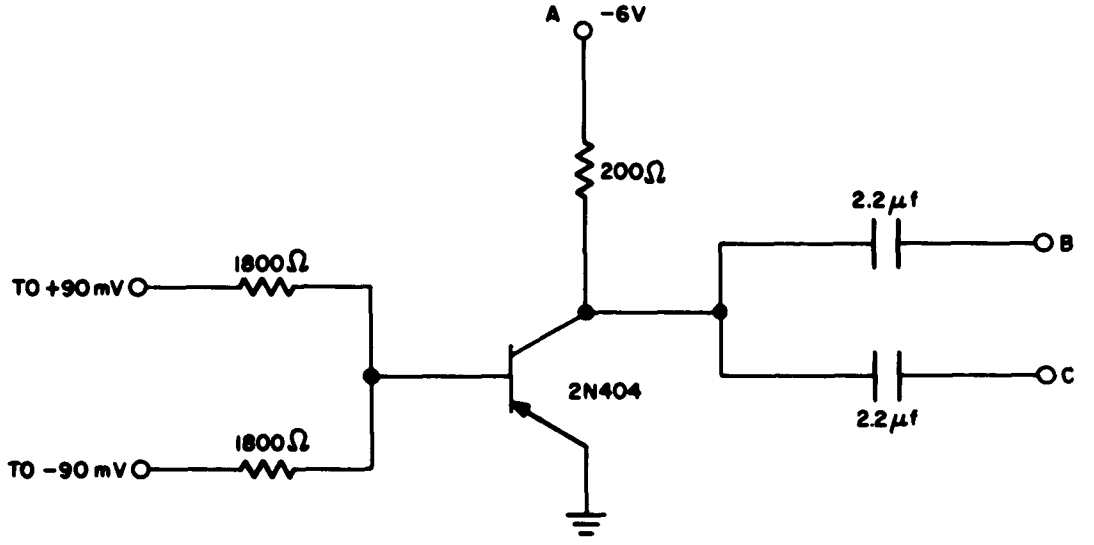


Figure 2-18. Transistor Switch for —6v Protection

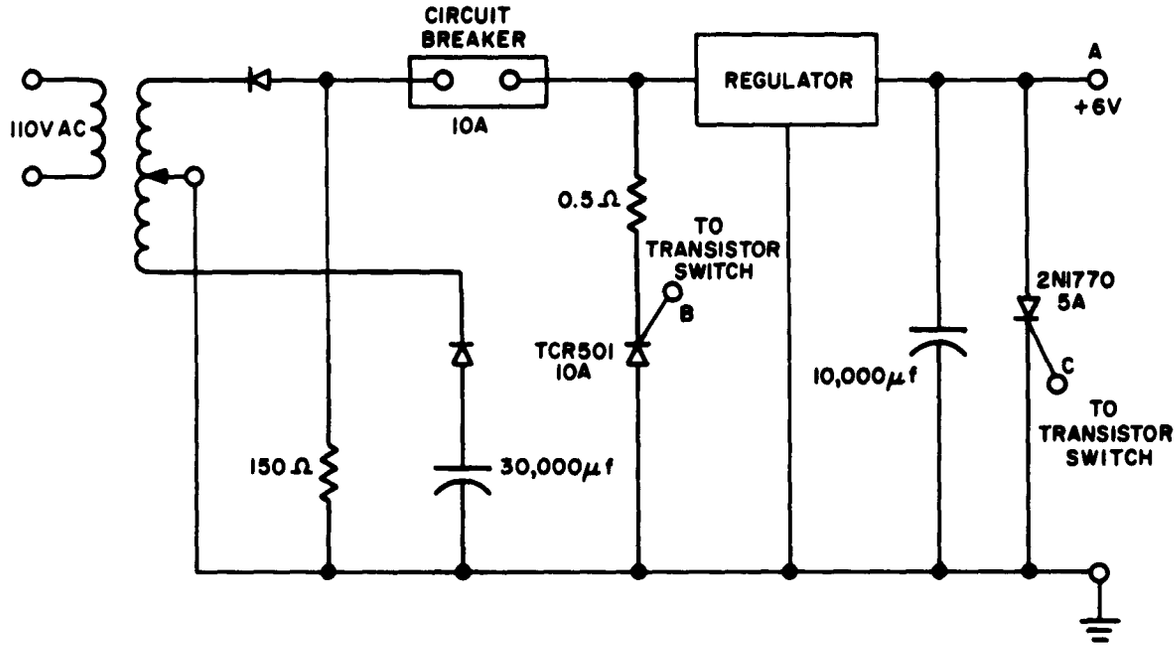


Figure 2-19. Protection Scheme for +6v Supply

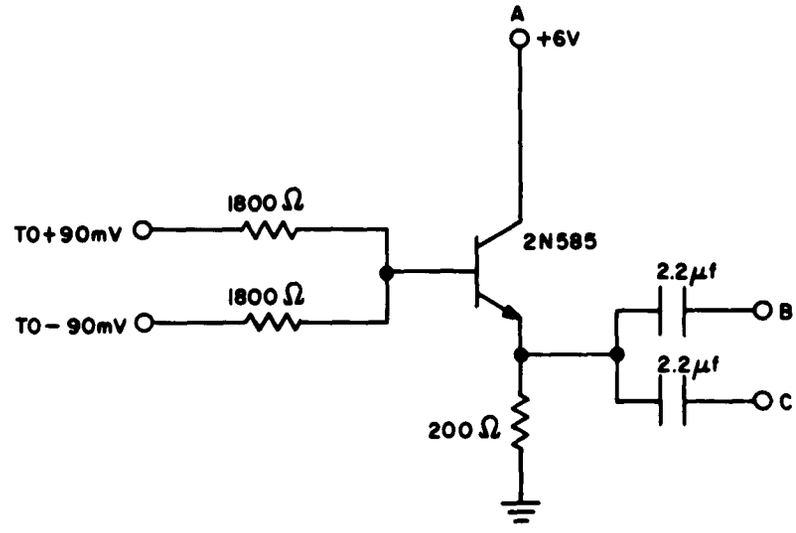


Figure 2-20. Transistor Switch for +6v Protection

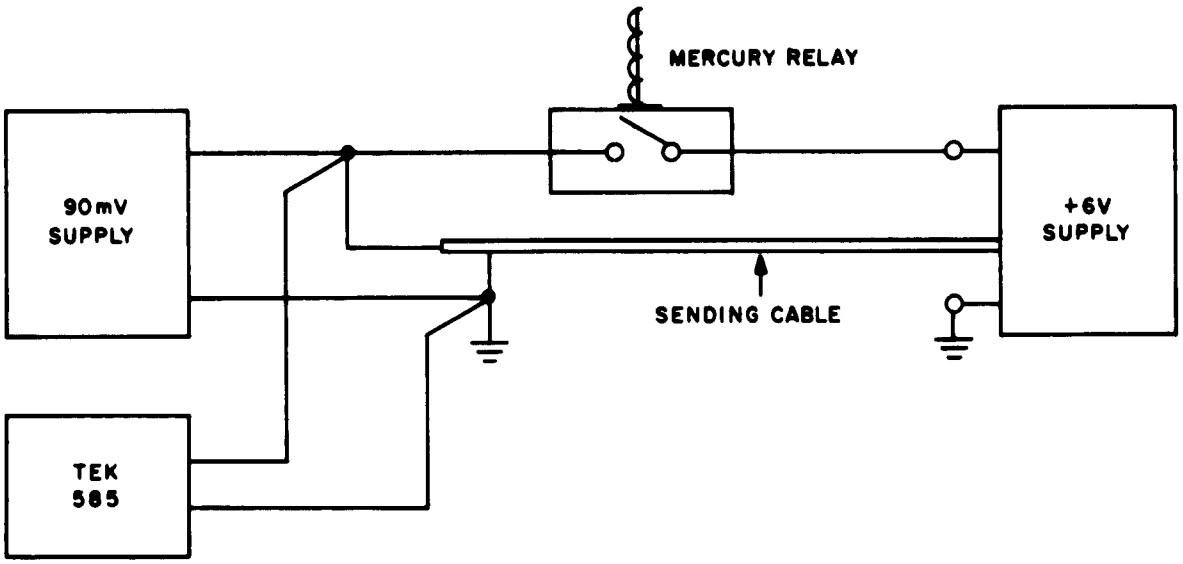


Figure 2-21. Transient Study Test Setup

The following facts were observed when only two wafers were operated. Some of these observations may have to be modified by the results of further experiments.

The results of these tests did not support the observations made on the A register test frame. The inconsistency was due to poor ground contacts due to probing, and deteriorated performance of the filter pad. The SKL tests immediately revealed that there is an under-damped resonant disturbance on the reset side of the bistable wafers at a frequency of 278 mc. The max. peak-to-peak value of this disturbance was 10 mv with a damping factor of approximately 0.09. The set side exhibited an oscillation at about 70 mc with a slight amount of the 278 mc ripple superimposed. The peak-to-peak value of this disturbance was 8 mv. On the low-impedance line itself, the disturbance noticed was about 2 mv which appeared like a ripple at 70 mc.

It was observed that on the reset side of the bistable wafers, the clamp diodes and an AND diode are situated at a certain distance from the filter pad. The lead length from these diodes to the filter pad was found to generate large spikes due to differentiation. This type of construction must be avoided in future machines.

When operating at 50 mc and 100 mc, essentially the same things were noted. Some effects were more pronounced due to the adding up of the undamped modes. This situation was very noticeable on the set side where at 50 mc, the disturbance appeared almost like a fundamental with peak-to-peak value of 8 mv, while at 100 mc, it appeared like a fundamental with peak-to-peak value of 5 mv. Under these conditions the 278 mc ripple was negligible. On the reset side, at 50 mc, the damped oscillation at 278 mc was the most prominent disturbance with a max. peak-to-peak value of 12 mv. At 100 mc, however, an irregular waveform of 15 mv peak-to-peak with a fundamental at 278 mc was evident.

The waveforms observed on the plug-in wafer were almost identical with those observed on the soldered-in wafer. The low-impedance line was observed to cause coupling of about 2 mv between adjacent wafers at a fundamental frequency of 50 mc. The 100 mc figures are not yet available.

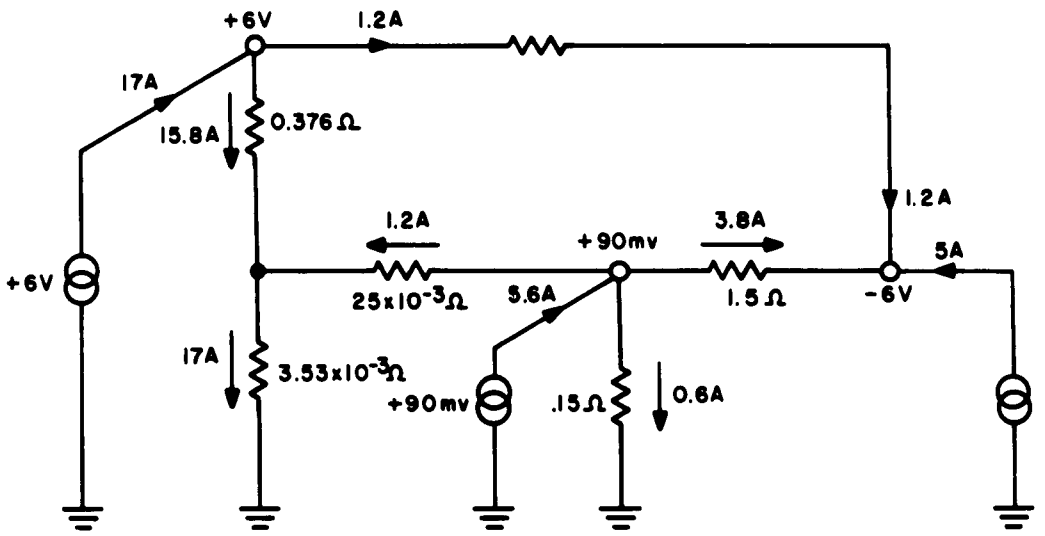
An attempt was made to change the resonant frequency of 278 mc to a much lower value by adding capacitance at the back of the wafer. This was done on the reset side with a piece of Hi-K material whose capacitance was approximately 12,000 pf. The disturbance waveform was changed after this addition but the peak-to-peak values were not reduced to any large extent.

3. Power Supply-Subsystem Interaction

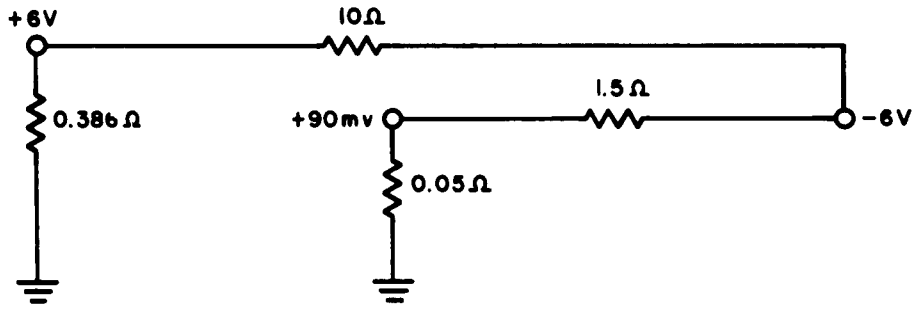
When all the units of the subsystem were placed in the main frame and the power was connected, it was found that the power supply would trip-off automatically. This was traced to the action of the overvoltage protection on the +90 mv supply. The main cause of this was later traced to an oscillation of about 150 mv at about 450 kc on the -6 v line. This oscillation was found to occur only when the subsystem was connected. External resistive loads connected across each of the power point were able to draw stable load currents. This seemed to indicate that the oscillation was caused by the currents flowing from one power point to another, especially from the +90 mv to the -6 v point as is the case within the subsystem. A resistance model of the subsystem as shown in Figure 2-22 was proposed. Such a simulated load is being built to determine whether the resistive model of the subsystem is the cause of the oscillation.

The oscillation was quenched by connecting a 3000 uf electrolytic capacitor across the -6 v point, which corrected the phase shift sufficiently to quench the oscillation.

Figure 2-23 gives a detailed account of the currents flowing and the d-c drops along the distribution lines.



(a) SIMULATED RESISTIVE LOAD ON POWER SUPPLY



(b) APPROXIMATION OF (a)

Figure 2-22. Resistance Model of Subsystem

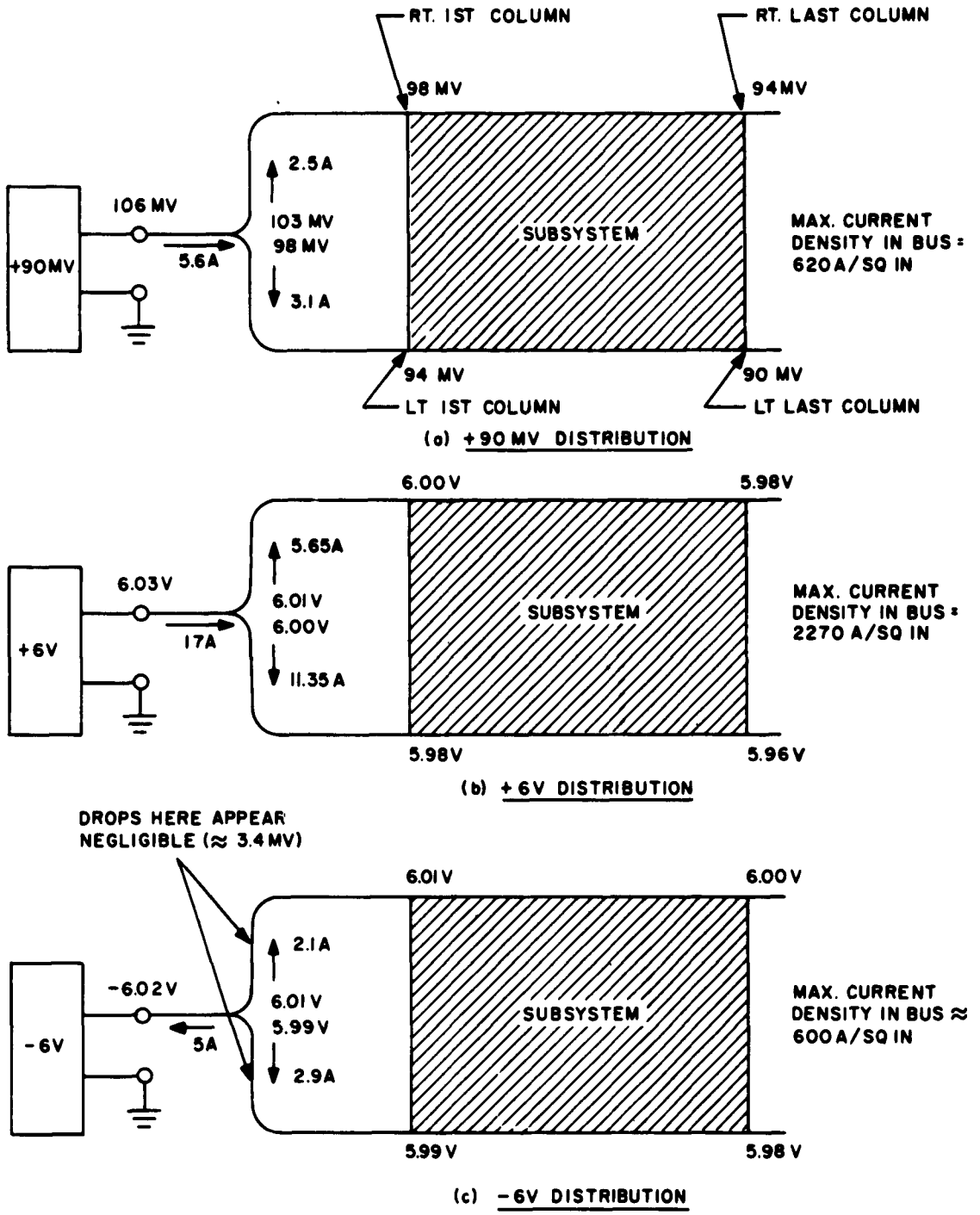


Figure 2-23. Current Flow and D-C Drops

Chapter 3. MEMORIES

SUMMARY

The 32-word 5-bit Memory Subsystem having parameters required for a 1024-word 24-bit memory was made operational this quarter and is undergoing final test. All words have been selected at a 33-megacycle rate. At this speed, the subsystem has indicated that the most significant time is the decode time. Decoding to one out of 1024-words without designing special decoding circuits resulted in a typical decode time for the subsystem of 30 nanoseconds.

The 24-bit words have been built, d-c checked, and are now being tested in the 9-word memory.

All 160 bits in the 32-word subsystem have held information without errors for periods of up to 3 hours. The subsystem is still being debugged with reliability improving. The major problem now appears to be mechanical intermittents.

The full decoder, still in the debugging stage, has operated for a maximum of 7 hours.

Chapter 3. MEMORIES

I. PERSONNEL

The following personnel contributed to this phase of the project during the fourteenth quarter:

G. Ammon
L. Dillon
M. M. Kaufman
J. P. McAllister
P. Palamar
J. Schopp
L. Wu

II. DISCUSSION

A. REVIEW

1. General

The all-tunnel-device memory proposed one year ago for Phase III-B of the LIGHTNING Program has been built and is undergoing final tests. This memory followed a four-year study of various memory types at both the RCA Laboratories and the Electronic Data Processing Activity. During two of the four years, all memory effort was placed on tunnel diode types. This direction was taken after tunnel diodes became the obvious choice for the high-speed switching element.

The first tunnel diode memory cell studied used one tunnel diode and two resistors. This cell was attractive from a minimum device point of view; however, drive magnitudes, tolerances, and sense amplifier gain requirements at LIGHTNING speeds made the cell difficult to operate successfully.

The next memory cell studied was a rectifier-coupled type which used two tunnel devices. The requirements on this cell were sufficiently realizable to make it the final choice.

The final system design chosen was word organized in order to minimize the sense amplifier requirements. All memory parameters in the final design were chosen on the basis of worst-case studies and for use in a 1024-word 24-bit memory.

The actual feasibility model built and now under test is a 32-word 5-bit memory with the drive voltage magnitudes, transmission line impedances, and tunnel device types required for a 1024-word system.

2. Memory Configuration (First Implemented)

Figure 3-1 shows that part of the memory designed and built first. The four-plane memory stack shown has been built in the laboratory to occupy the same volume that the 1024-word stack would occupy. The line impedances and terminations are at the magnitudes required in the larger memory and all drive circuitry therefore is capable of handling a 1024-word memory. Each plane has dimensions and transmission line lengths corresponding to a 32 by 24 bit plane; however, only 8 words by 5 bits are installed per plane in the 32-word memory.

During the memory cycle, a word driver is selected by a word switch in the selection matrix or second level decoder. The "1" output from the memory drives the sense amplifier which, during the read regenerate cycle, switches the digit drivers via the regeneration loop and regenerates the information.

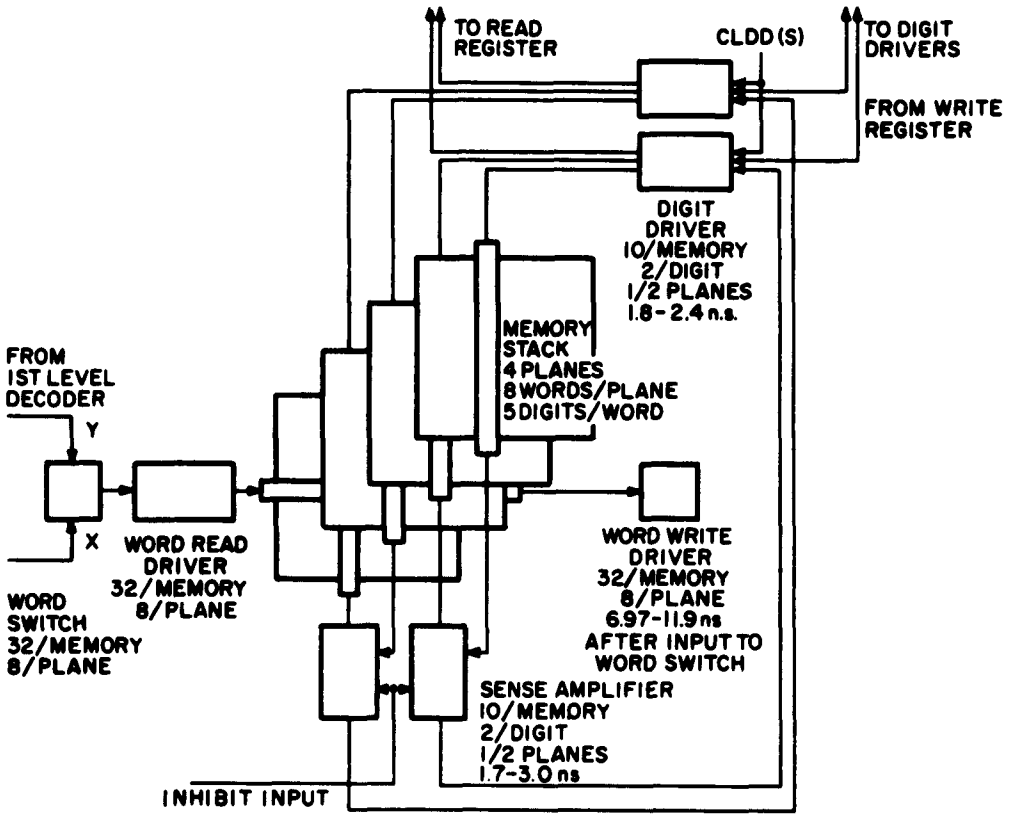


Figure 3-1. Partial Memory Block Diagram

The sense amplifier is inhibited by the Logic Subsystem during a write cycle and information is fed into the digit driver from the Logic Subsystem. The digit driver produces a level output to insure worst-case coincidence between the word drive jitter and digit drive. The write driver is triggered by the trailing edge of the read pulse and therefore writing is very closely timed with respect to reading.

3. Memory Configuration (Second Implemented)

The remaining parts of the Memory Subsystem are shown in Figure 3-2. These include the timing generator, the memory address counter, the first level decoder, and buffer circuits required to combine the Logic and Memory Subsystems. Except for the timing generator, these portions of the system involve general logic functions, and have been built with the standard logic circuits used in the Logic Subsystem. In a few cases, they are modified to suit custom requirements. The logic circuits were built on wafers and placed in wafer frames which are located around the memory.

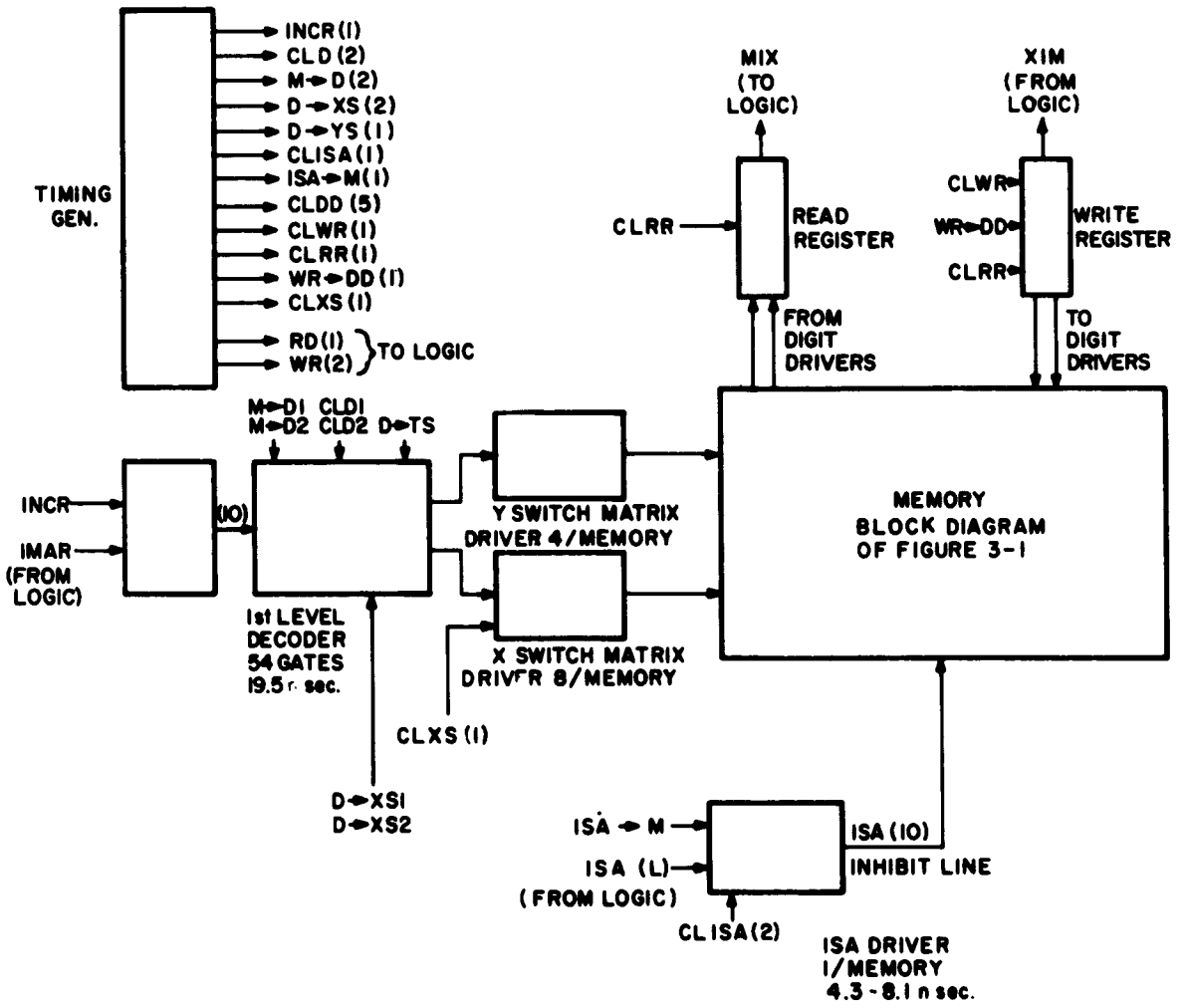


Figure 3-2. Complete Memory Block Diagram

The memory is now being operated synchronously, clocked by a snap-off diode timing generator. The timing generator develops 22 logic pulses and delivers them to the system through the required worst-case delay. All timing pulses are identical to logic circuit pulses and the timing generator therefore can be replaced by a logic circuit control unit and the memory operated asynchronously on demand by the Logic Subsystem.

The combination circuits are required between the logic and memory to allow synchronous operation of the memory and asynchronous operation of the logic. They also invert the positive pulses from the logic into the negative pulses required by memory, and vice versa.

4. Memory Times

Table 3-1 indicates memory times which are minimum, typical, and maximum times corresponding to the significant memory operations.

TABLE 3-1
MEMORY TIMES

Memory Function	Time In Nanoseconds		
	Minimum	Typical	Maximum
Full Decode (1/1024) + Read	33.6	36.6	45.4
Full Decode (1/1024)	28.0	29.7	34.9
Difference	5.6	6.8	10.5
Full Decode (1/1024) + Write	34.3	37.0	45.9
Full Decode (1/1024)	28.0	29.7	34.9
Difference	6.3	7.3	11.0
1024-Word Decoder			
1st Level Decode	17.1	17.8	20.2
2nd Level Decode	10.9	11.9	14.7
Total	28.0	29.7	34.9
32-Word Decoder			
1st Level Decode	6.8	7.2	8.1
2nd Level Decode	4.2	4.6	5.7
Total	11.0	11.8	13.8

The full decode time plus the read time can be considered a complete demand cycle because the decode time is considerably longer than the sense amplifier recovery time. The sense amplifier recovers from the digit disturb 7 nanoseconds after the read pulse. The typically 30 nsec decode time more than overlaps the recovery time. The full decode time for decoding one out of 1024 words is shown in Table 3-1 and is the time used in the 32-word system to simulate decoding one out of 1024 words. The times only associated with driving and sensing the memory cell which are the differences between rows one and two in Table 3-1 are considerably less than the full decode time. The decode plus write time is approximately the same as the read time with the sense amplifier recovery again not a limiting factor. The sense amplifier recovery which includes the regeneration time becomes a limiting factor in both the read and write operation only when the full decode is less than 7 nanoseconds.

It is now realized that the most significant time at these speeds is the decode time. To reduce the decode time, more gain should be given to the word drivers and all power required for the decoder to minimize its transit time should be allowed.

The 32-word memory which simulates decoding to 1024-words has decoder circuits at the higher power levels and most of the gain between the logic circuit drive as well as the word drive is accomplished in the decoder. Reducing the number of words allows the selection matrix or second level decoder to be driven at lower power levels. Table 3-1 also indicates the 1st and 2nd level decode times required for only a 1024-word and 32-word decoder.

The maximum cycle time for the 32-word memory without simulation to a larger memory would be 10.5 μsec memory time + 13.8 μsec decode time or 24.3 μsec.

5. Memory Circuits (Other Than Logic Circuits)

The circuits required in the Memory Subsystem other than the standard logic circuits are shown in Figures 3-3 and 3-4. There are eight such circuits; the memory cell, the read driver, the write driver, the pre-amplifier, the sense amplifier, the digit driver and the timing generator.

The timing generator (Figure 3-3) produces a maximum of 24 logic pulses of which the memory utilizes 22. The basic operation of the snap-off diode uses the sharp cut-off characteristic of minority carrier flow through a conventional rectifier junction.

The word switch (Figure 3-3) which makes up the selection matrix or second level decoder is basically a rectifier switch. A 50-milliamp GaAs tunnel diode is selected by a Ge tunnel rectifier. The X plus Y inputs exceed the rectifier voltage threshold and select the diode. Voltage selection allows 64 AND gates or switches to be driven by one output.

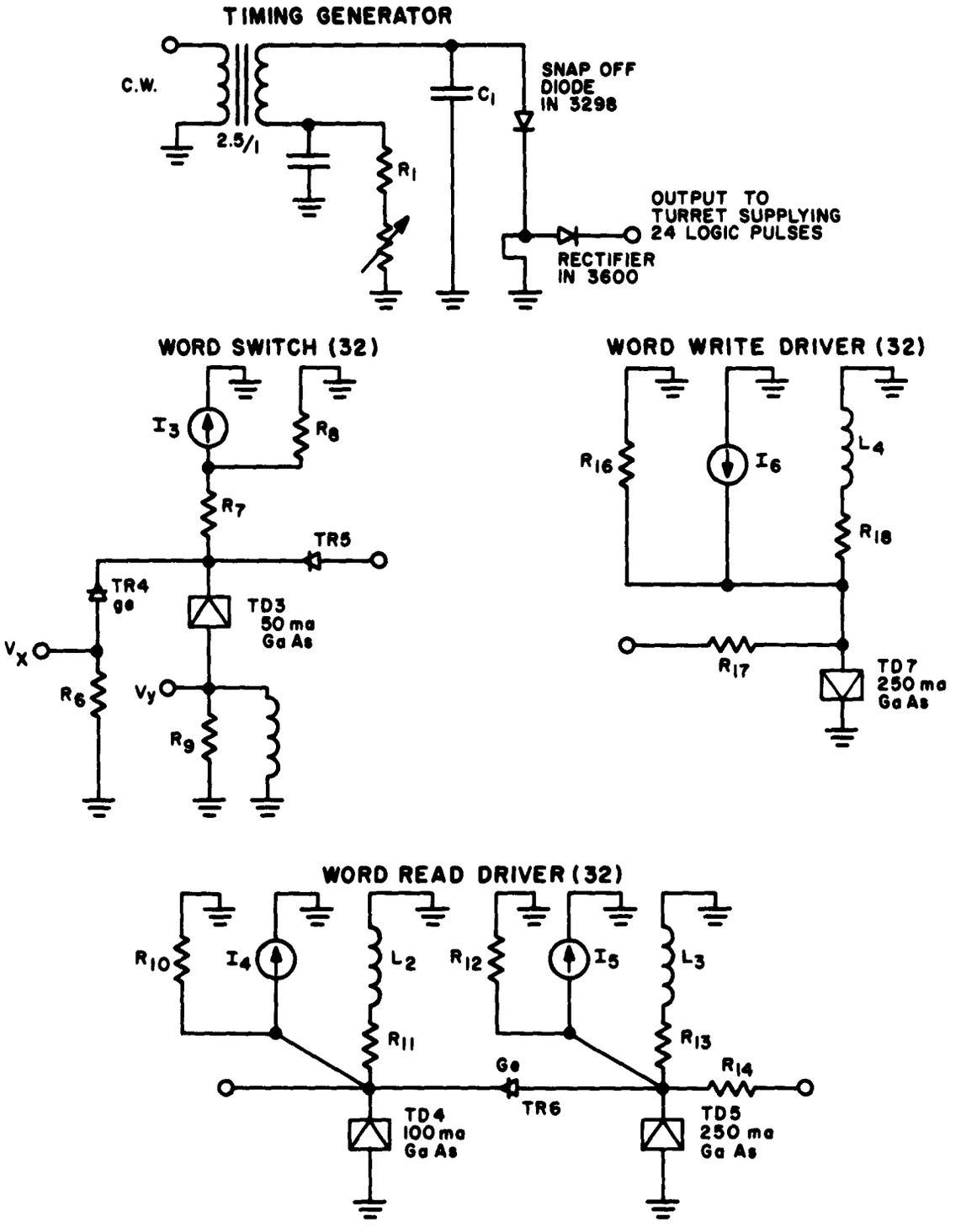


Figure 3-3. Memory Circuits

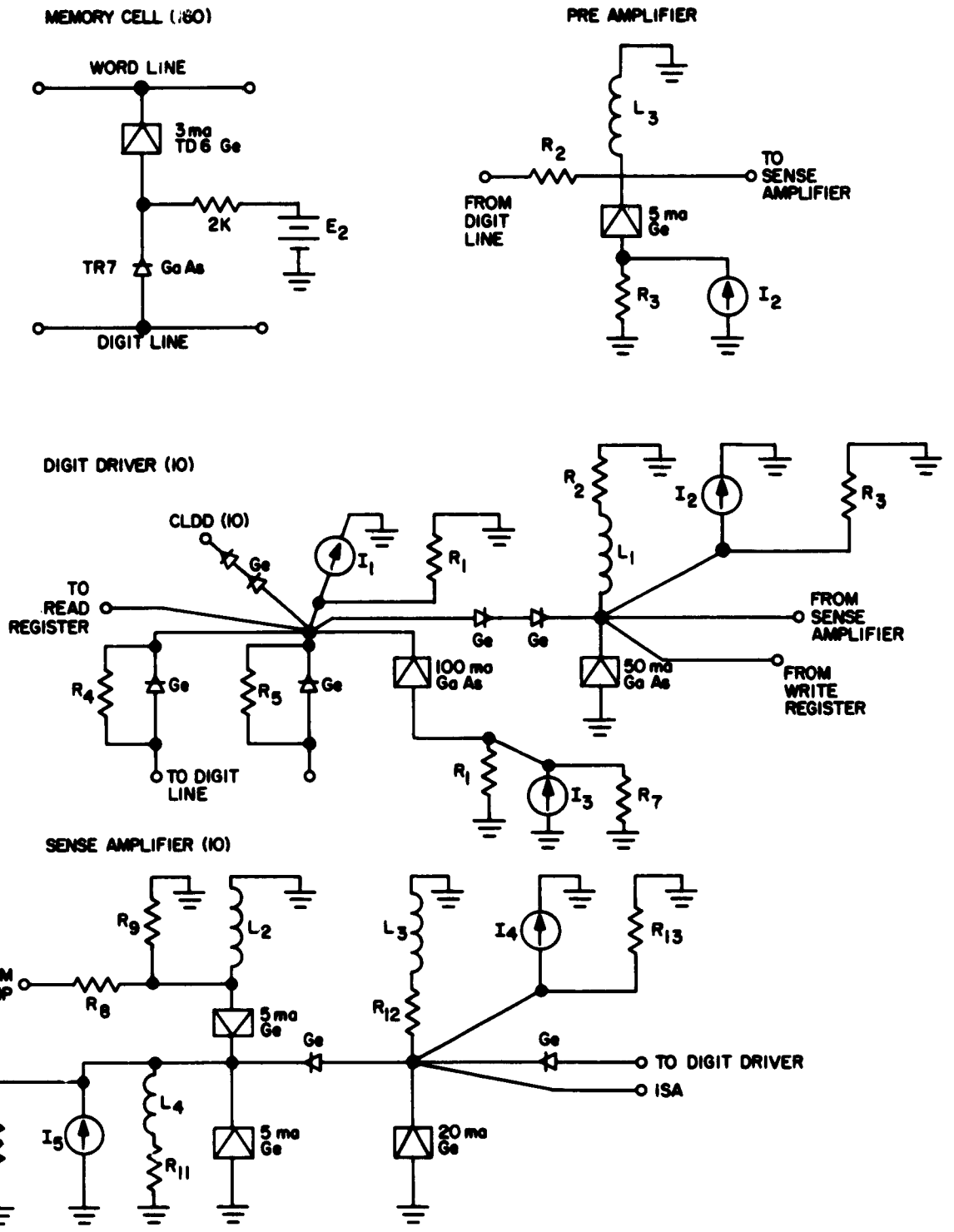


Figure 3-4. Memory Circuits

The read driver (Figure 3-3) is selected by the word switch and provides the additional gain required to drive the word line.

The write driver (Figure 3-3) is driven by the trailing edge of the read pulse through the word line. The output is therefore always very closely related in time to the read pulse.

The decoder supplies approximately five times more gain between the logic and memory than the read driver. A redesign of this circuit for a higher gain read driver would minimize the decode time.

Figure 3-4 shows the remaining memory circuits.

The memory cell uses a 3-ma peak current Ge tunnel diode and a GaAs tunnel rectifier. The tunnel diode is rectifier coupled to produce the highest output available from a tunnel diode cell. The rectifier coupling also permits driving a tunnel diode cell with the lowest possible drive voltages.

For historical reasons, a positive bias is used in the cell, the output signals are negative pulses, and the drives required are negative. To combine the Memory and Logic Subsystems, pulse inverters are used. A redesigned cell would use a negative bias voltage in the cell and reverse all tunnel devices to allow positive devices. The inverters between logic and memory would then be eliminated.

The pre-amplifier was the only circuit whose operating conditions were sufficiently difficult to predict because of the many sources of noise input. Therefore, this circuit was not worst-case simulated on a computer. The pre-amplifiers are individually biased and can sense 32 bit lines.

The sense amplifier supplies the additional gain required to switch the digit driver. It also has an inhibit input which allows the logic to clear the memory word during a write cycle.

The digit drivers supply the remaining gain required to drive two digit lines or 64 bits. GaAs stages are used to develop the voltage required to drive the memory cells and allow a partial termination at the input to the lines.

Table 3-2 gives the memory circuit tolerances. The first column indicates the memory circuit type and the second column indicates the tightest tolerances on the circuit as determined by the worst-case computer simulation. The last column indicates the working range measured in the laboratory. As indicated, the pre-amplifier was not simulated on a computer.

The ratio between the tolerances in the last two columns, if all conditions were simulated in the laboratory, should be larger in a number of places. Possibly this is due to some undetected, out-of-specification components in the system.

TABLE 3-2
CIRCUIT TOLERANCES

Circuit	Computer Simulation Worst-case Voltage Bias Tolerance	Laboratory Working Bias Range In System
Word Switch	±2%	±4.1%
Word Read Driver	±3%	±6.5%
Word Write Driver	±3%	±2.2%
Memory Cell	±2%	±7.4%
Digit Driver	±3%	±2.3%
Sense Amplifier	±2%	±4.1%
Pre-Amplifier	Not Performed	±1.3%

The working ranges show that the tightest tolerance on the pre-amplifier is ±1.3%. It is believed, assuming that stable resistors and power supplies are used, these ranges are sufficient to allow reliable operation.

6. Main Frame

The picture of the main frame, shown in Figure 3-5, indicates the relative position of all blocks in the memory system. The memory stack, drive and sense circuits are not on wafers. However, the required logic circuits are on wafers placed around the stack in frames.

The address counter and first level decoder is shown at the appropriate height to drive into the second level decoder or selection matrix.

7. Individual Blocks

Figure 3-6 is a close-up of the memory stack. This stack was built and tested in two identical halves with each half having its own set of drive and sense circuits. The halves are connected with the foot arrangement shown. The stacks were considered operational only when the working voltage ranges correlated to the worst-case simulation studies and were sufficiently large to insure reliable operation.

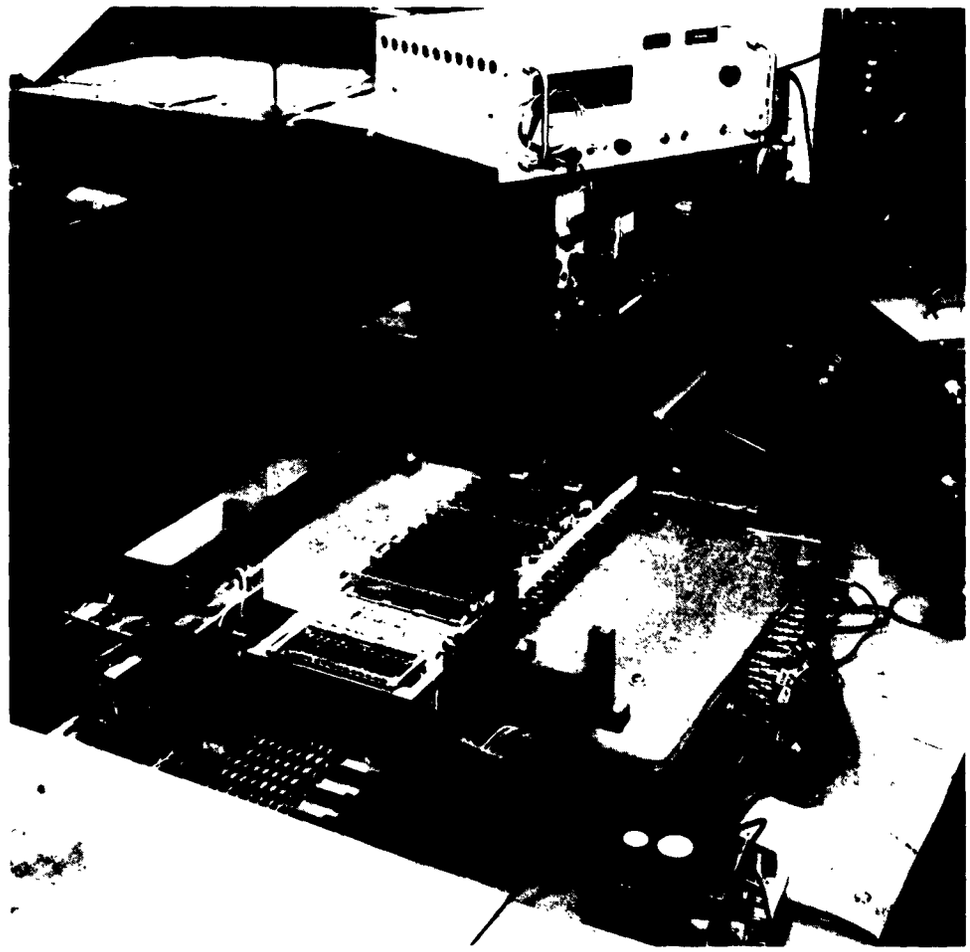


Figure 3-5. Memory Main Frame

Figure 3-7 shows waveforms generated by the stack under specific information conditions. The stack was loaded with fixed information, which when viewed during continuous read out in the regeneration loops, resulted in the pulse pattern shown. Each pulse is the sum of one digit in a word with the minimum pulse indicating the minimum number of "1's" in that word.

Figure 3-8 is a close-up of the timing generator which, as indicated, has one snap-off diode driving 22 delay cables for memory. The delay cables have 50-ohm impedances and have been individually wrapped and placed in the slots shown. The maximum output from the snap-off diode is 35 volts which is reduced in the distribution turret to logic pulse amplitudes.

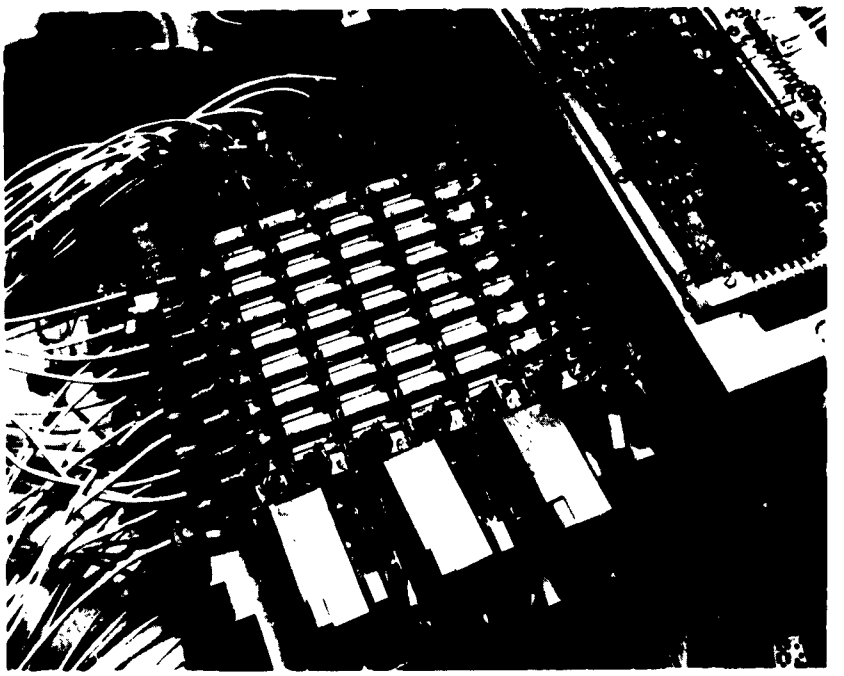
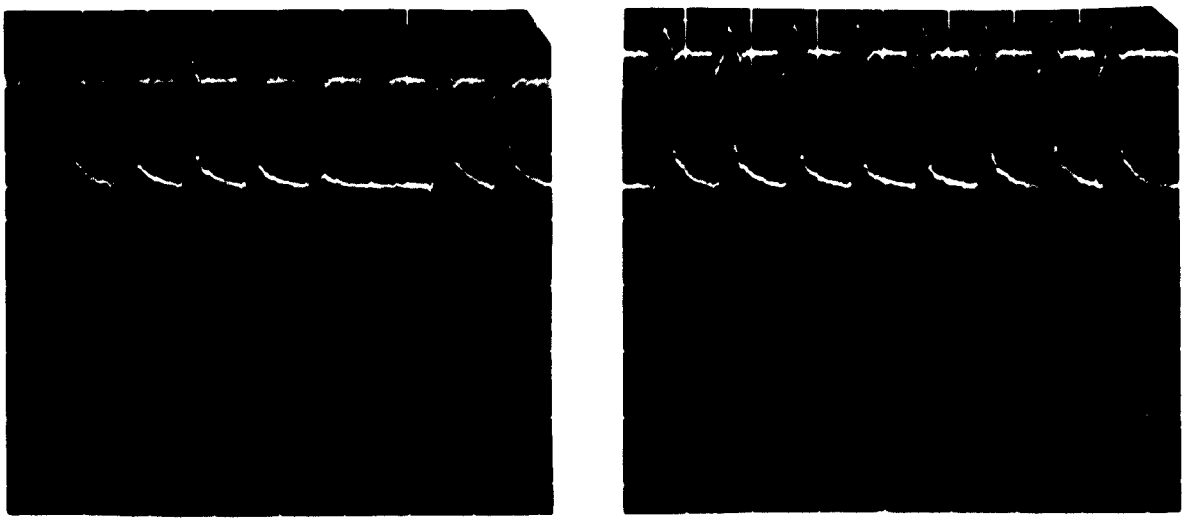


Figure 3-6. Memory Stack



30 NS/DIV
WORD DRIVE (TOP)
MEMORY INFORMATION PATTERN A
(BOTTOM)

30 NS/DIV
WORD DRIVE (TOP)
MEMORY INFORMATION PATTERN B
(BOTTOM)

Figure 3-7. Memory Information Patterns

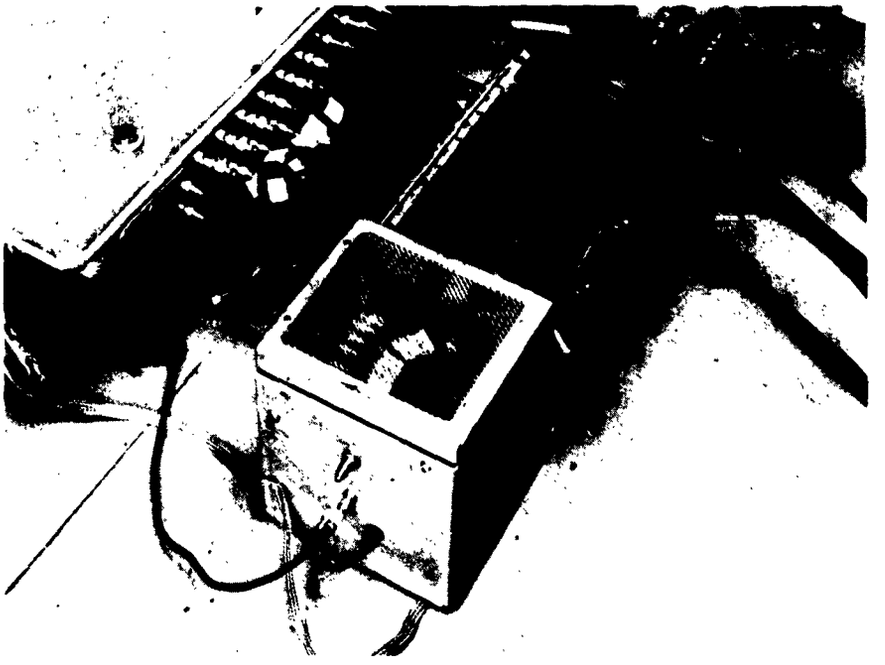


Figure 3-8. Timing Generator

8. Difficulties Encountered and Overcome

A major difficulty encountered early in testing the memory stack was related to the tunnel rectifier d-c characteristic. The rectifier which is a very low peak current tunnel diode was originally assumed to have a high impedance in all its non-conductive regions. However, it was found that the rectifiers tunneling characteristic allowed the dynamic impedance close to the origin to be much lower than anticipated. The memory cells originally were designed so that in the one stage the tunnel rectifiers were biased close to the origin.

The memory lines under this condition were very lossy to memory cell outputs and the lines were almost impossible to sense. The design change required was a shift in the bias voltage on the digit line. The corresponding effects on all circuits involved were then included in the worst-case computer simulations.

The other major difficulty throughout the memory testing was cross coupling between circuits, and particularly, noise fed over to the sense amplifier. This problem required careful shielding of the sense amplifiers and digit drivers. The ground currents also had to be carefully isolated.

9. Extensibility Words

There have been two words constructed of 24 bits each to be installed in the 32-word system to prove the extensibility of the system to larger size. These words, shown in Figure 3-9, have been completely d-c checked.

10. Nine-Word System

The nine-word system is being tested at a 65 megacycle repetition rate to indicate the repetition rate potential of the basic memory cell. The modifications required were on the sense amplifier and digit driver. These involved non-linear biasing of the tunnel diodes to insure a minimum recovery time.

The sense amplifiers have been driven at approximately 150 megacycles indicating less than 5 nanoseconds recovery time.

11. Conclusions

A 32-word 5-bit memory with parameters required for a 1024-word 24-bit memory has been constructed and is under final test.

The memory is working, but testing and debugging is not yet complete. Testing to date of the individual blocks and the overall system operation indicates that reliable operation should be achieved after debugging.

The 32-word memory subsystem has shown that tunnel diode memory cells can be operated at repetition rates of 32 megacycles and in the 9-word system as high as 65 megacycles. The system has indicated that, at these speeds, the most significant time is the decode time. To decode to one out of 1024 words without designing a special circuit type for decoding has resulted in a typical decode time of 30 nanoseconds for the subsystem.

Using the techniques developed on the LIGHTNING Program, a small B-box memory could be designed with a decode read and regenerate time of 25 nanoseconds and with a typical decode plus read time of 15 nanoseconds.

The memory considering all peripheral hardware, can be built at about three tunnel devices per bit and for those applications where short access time is required, the memory serves a useful purpose.

B. MECHANICAL CONSIDERATIONS AND TIMING

1. Main Frame Assembly

The main frame for the Memory Subsystem consists of a supporting structure, a power distribution system, a cooling system, an interconnection scheme for the logic components, the console, timing generator and the memory stack. The logic components are the decoder, counter, X and Y switch matrix driver, inhibit sense

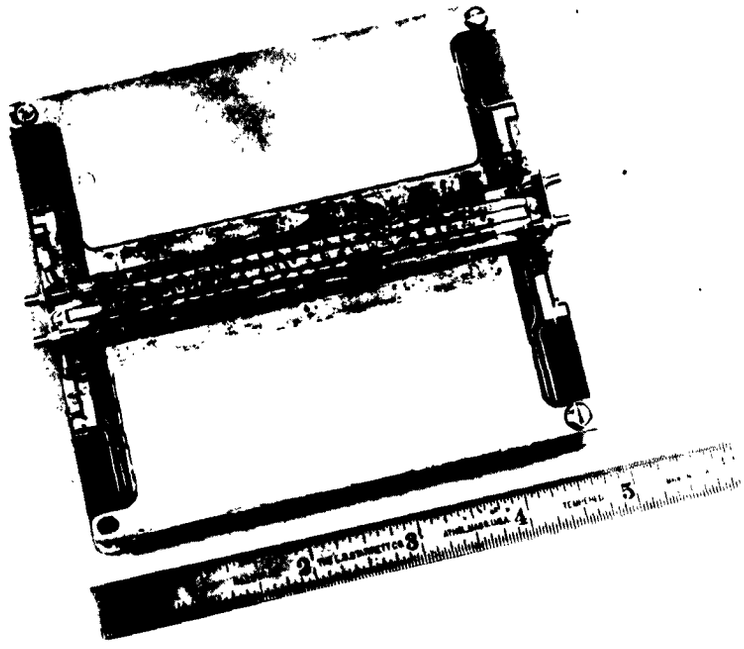


Figure 3-9. (a) Word and Power Supply Lines for the Memory Extensibility Plane

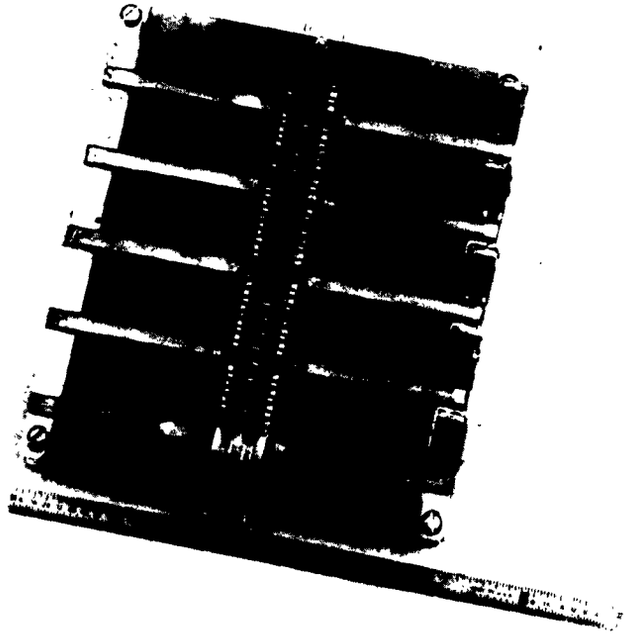


Figure 3-9. (b) Digit Lines and Preamps for the Memory Extensibility Plane

amplifier driver and the read and write registers. The memory stack is comprised of the cells, digit drivers, sense amplifiers, the word switches, and word read and write drivers.

2. Supporting Structure

The supporting structure for the logic components consists of a table with two levels above and two levels below. The levels below are used for the memory stack power supplies, the console power supplies and the air conditioner. The memory stack is supported on its own mount which rests on the table top. The first level above the table top contains the memory address decoder and counter. The second level supports the five power supplies for the memory peripheral system. The table is functional in terms of allowing accessibility to all four sides and is designed such that it can be lifted by a conventional fork lift truck for mobility.

3. Power Distribution

The power distribution for the memory stack is obtained by using constant-current resistor brackets and converting to a voltage source on the circuit by going through a very small resistor. This technique provides an electrically simple means of d-c power distribution. However, for the peripheral circuits (decoder, counter, XSMD, YSMD, ISAD, and read and write registers), a distribution system simular to that of the Logic Subsystem was chosen. This method provides a constant voltage source to the wafer. The distribution for the power supplies to the I beams is accomplished through low inductance copper clad power buses. This bus is a newly developed "IRC" power strip consisting of four conductors (10-mils thick) on a 10-mil copper back separated by 5 mils of mylar dielectric material. A special coaxial stud was developed and installed on punched holes made on power strip. The four conductors represent from top to bottom -90mv, +90mv, +6 volts and -6 volts. Although only four voltages were required, a fifth power supply was necessary to provide the 6-volt current requirements.

4. Interconnections

Interconnections for the Memory Subsystem are as follows:

Wafer-to-Wafer Connections - Most of these connections were made with 25.7-ohm extruded copper coaxial cable. However, there were some applications for 5-ohm extruded copper coaxial cable.

Inter-Frame Connections - These connections were made exclusively with a 25.7-ohm flexible cable by means of a solder down type connector.

Timing Generator Connections - The 50-ohm output cables of the timing generator connect to a panel on counter decoder level. From this panel, these cables are connected to their associated wafer frames by means of the solder down type connector.

Console Connections - Each of the 42 bistables throughout the memory peripheral system has its state displayed by a console light. This is accomplished through a high impedance on the bistable diode feeding a 25.7-ohm coax to a console connection panel on the decoder counter support. From this panel, a seven-foot 50-ohm cable connects the signal to the console. At the console, it is possible to set, reset, display and master clear the bistable.

5. Cooling System

The cooling system for the Memory Subsystem was initially designed such that "muffin" fans would be sufficient. However, with the advent of the plug-in wafer, the air flow was somewhat restricted. Higher capacity fans were successful in eliminating this problem. When the entire subsystem was assembled, an air conditioner was installed below the main frame table to provide the fans with cool air, since the ambient temperature of the building varied over too wide a range.

6. Memory Subsystem Timing

The Memory Subsystem is timed by 22 clock pulses obtained from a timing generator. This generator consists of a snap-off diode pulse circuit driving different lengths of cable to obtain the proper delay. These clock pulses are shown in Figure 3-2 and are defined below.

CLD1, CLD2: Clear decoder bistables to quiescent state (high state)

M→D1, M→D2: Start decoder. Transfer the contents of the memory address counter to the decoder.

INCR: Increment the memory address counter when enabled by the Logic Subsystem signal (IMAR).

WR1, WR2: Input to Logic Subsystem control which in turn initiates a clear-write cycle in the Memory Subsystem.

CLWR: Clear write register to all "0"'s.

ISA→M: Inhibit the sense amplifiers when enabled by the Logic Subsystem signal (ISA).

D→XS1, D→XS2: Clock decoder X output into X switch matrix driver.

D→YS: Clock decoder Y output into Y switch matrix driver.

CLDD1 thru CLDD5: Clear memory bistable digit drivers.

CLRR: Clear the memory read register.

WR—►DD: Transfer the contents of the write register into the memory digit drivers.

CLXS: Clear the X switch matrix driver bistables to quiescent state (low state).

CL/SA: Clear the inhibit sense amplifier bistables to the low state.

RD: Input to Logic Subsystem control to initiate a transfer from the memory read register to the logic X register.

The spread between these clock pulses is obtained by considering the worst-case transit time minus the best-case transit time of the next clocking signal. After the spread between associated clock pulses is found, the entire subsystem timing can be obtained by tabulating the spreads between all clock pulses using the first clock pulse as the reference. This timing is shown in Figure 3-10.

C. WORD SELECTION MATRIX (2ND LEVEL DECODER)

1. General

The matrix driver circuits (X and Y drivers) and the CLXS reset amplifier have been integrated into the Memory Subsystem. A description of each of these circuits and their logic function was given in IRR-13A. Also included were circuit schematics and an explanation of their electrical characteristics.

Six reset amplifiers, five CLDD's in the Y driver frame and one CLISA in the X driver frame are installed but will not be utilized until the combination circuits are installed.

2. System Description

An understanding of the overall system function of the selection matrix driver circuits can be obtained by studying Figure 3-11. The output stages of the X and Y drivers and the CLXS reset amplifiers are shown. The X driver (XSMD), a negative polarity bistable, is coupled to the word switch through an 8-ohm microstrip transmission line and a reverse biased "clamp" rectifier. The Y driver (YSMD), a positive monostable, is coupled to the opposite side of the word switch through a 2.5-ohm resistor and a 5-ohm microstrip transmission line. Common to all XSMD's is a 5-ohm microstrip transmission line through which the CLXS amplifier applies a positive polarity reset pulse on each cycle. A series parallel arrangement of four clamps is shown as the coupling element. This allows reset current to be drawn by that X switch which is set. Only one X switch will ever be in the high state since one word is selected at a time.

The figure shows only the intersection of one X and Y line with a word switch. The biasing networks for the diodes and coupling to preceding or succeeding stages,

as in the case of the word switch, have been eliminated on the figure to keep it relatively uncluttered. Actually the intersection of eight X lines and four Y lines define the positions of the 32 word switches. At the time coincidence of a negative level from an XSMD and a positive pulse from a YSMD, one of the 32 words is selected by the AND operation of the word switch. Before another word can be selected a pulse from the timing generator (CLXS) is amplified by the reset amplifier and used to reset the XSMD.

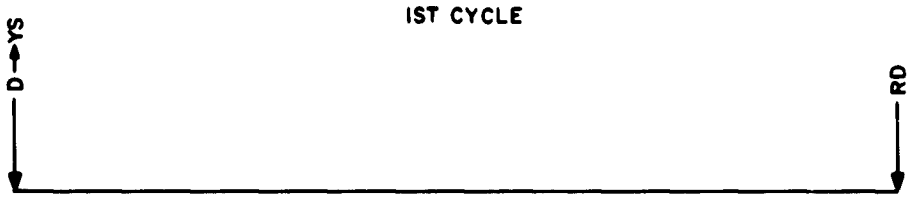
3. Power Distribution Difficulties

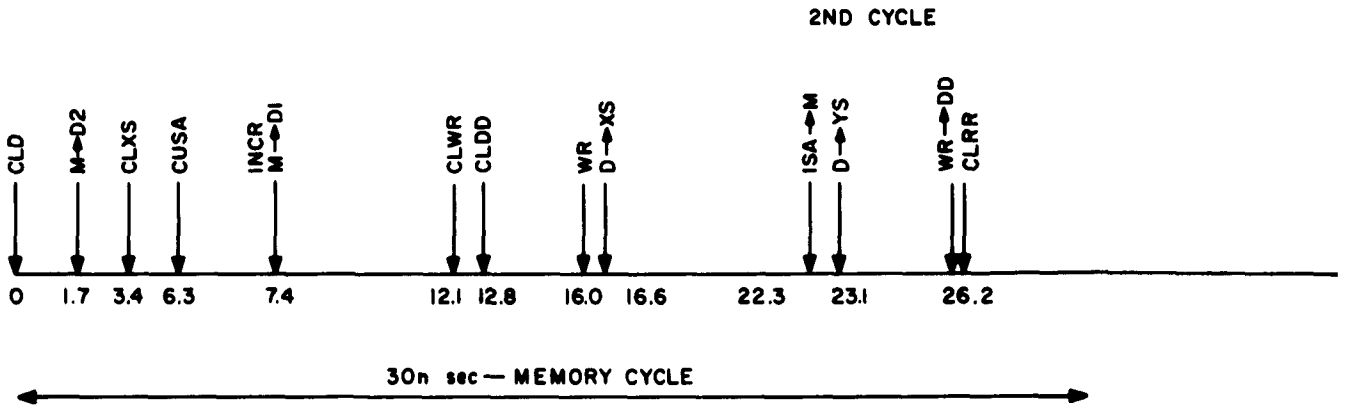
During the initial operating phase of the X and Y driver frames, permanent signal connections to the decoder and power supply connections to the distribution network were not used. The purpose was twofold in that it allowed these circuits to be located at a greater distance from the decoder thus increasing their accessibility for ease in troubleshooting. Also it was possible to disconnect from the decoder and use a signal generator for rapidly isolating troubles.

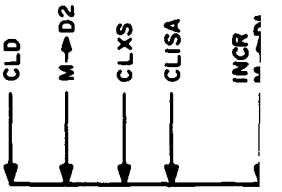
Since the permanent low-impedance distribution lines were too remote to be used, it was necessary to route relatively high d-c resistance (approx. 0.6 ohm) lines to a separate table which held power supplies. Under these conditions a considerable amount of difficulty was experienced in maintaining regulation of the +90 mv constant-voltage source. It was impossible to simply turn on the voltage to XSMD; instead, the voltage had to be increased slowly while each source was closely monitored.

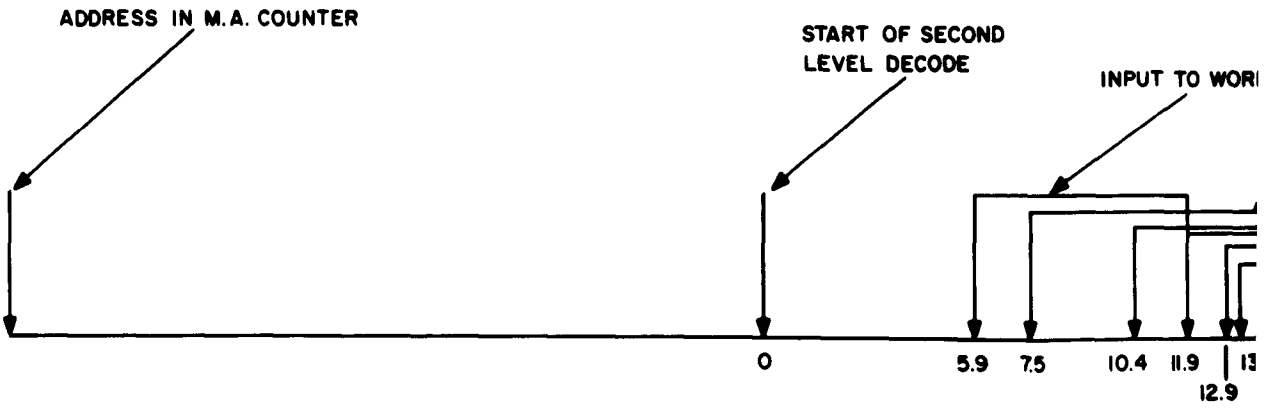
The reason for the difficulty can be seen from Figure 3-12 which shows a typical germanium amplifier stage. The +6V source and the 141-ohm resistor form a constant-current source which normally biases the tunnel diode near its peak. However, in the case of a disturbance caused by probing or some faulty circuit action it can be assumed that one or more Ge stages switch to the high voltage stable state. The tunnel diode now absorbs about 1/10 the current from the constant-current source and the rest is diverted through the clamp rectifier. The +90 mv source cannot regulate the voltage at the clamp because of the 0.6-ohm resistance and a large voltage drop occurs on the line between the clamp and the supply. This puts all clamps at about +300 mv. As a result all stages which have this +300 mv common point switch to the high voltage state and remain there.

Occasionally it has been found even with the permanent power supply methods that regulation is lost on the +90 mv supply. This is evidenced when the ammeter on the supply swings in the negative direction. Fortunately it is possible to simply shut all supplies off and switch them back on again with a resultant minimum loss of time.









2ND CYCLE MEMORY OPERATIONS

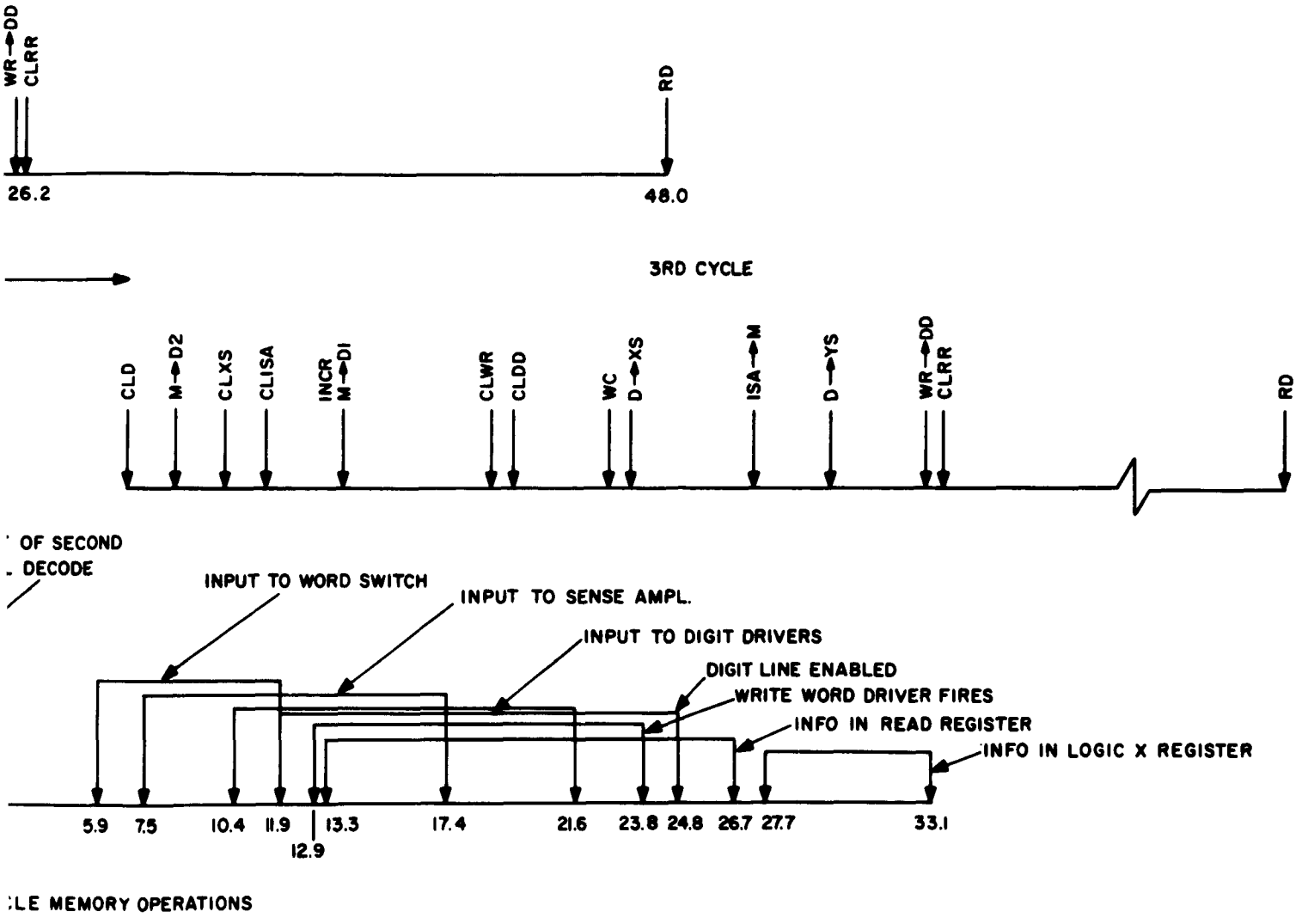


Figure 3-10. Memory Subsystem Timing

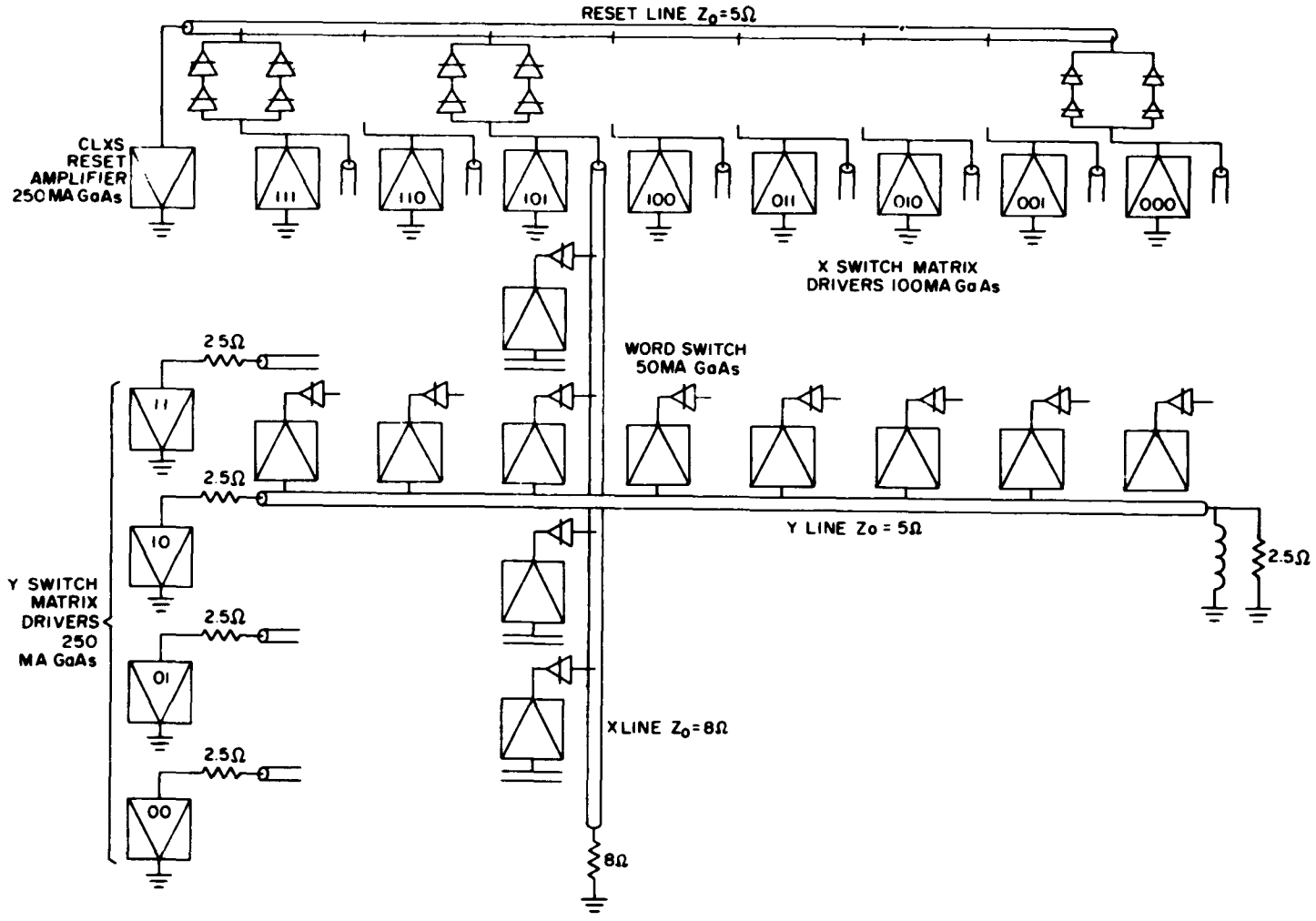


Figure 3-11. Matrix Driver Circuits

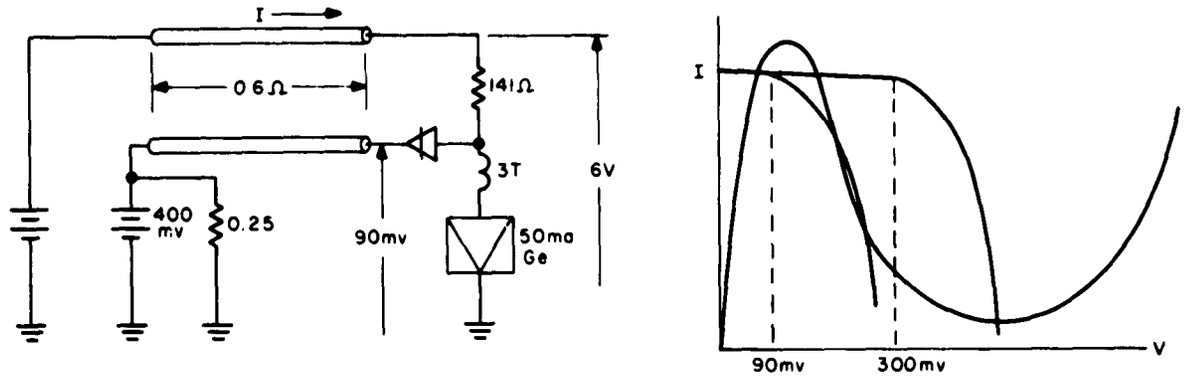


Figure 3-12. Temporary Power Supply System

4. Operational Difficulties

Initial operation of the matrix driver circuits demonstrated satisfactory performance. The circuits are capable of operating the 32 word switches with a ± 7.2% tolerance on the X switch and ± 2.4% tolerance on the Y switch power supplies.

One initial difficulty was very poor tolerance on the X switch power supply. The range was limited by double firing of word switches on the high side and inability to fire word switches on the low side. An oscilloscope display of the X switch output waveform showed the bistable was being set immediately after it was reset causing more than one word to be selected simultaneously. The difficulty was caused by coincidence of a negative reflection on the reset line and firing of the word switch into the X line. When current from both of these sources flow into the X switch, the resultant pulse is sufficient to switch the diode once again to the high voltage state. This condition was remedied by delaying the reset (CLXS) pulse an additional 1.5 nsec, thus removing the coincidence of the negative reflection and word switch pulse at the X switch and increasing the power supply range at the upper limit.

D. 32-WORD SUBSYSTEM TESTING

1. General

The Memory Subsystem was made operational this quarter with all parts assembled on the main frame.

2. Operation

A two-shift effort during the last month of the quarter allowed sufficient system debugging so that the full decoder can now select all locations at a 33-mc rate. All words (160 bits) have been read and regenerated at this rate. The system

is still being debugged to increase reliability. All 160 bits have held information without errors for periods up to 3 hours. There are 2 digit lines (16 bits) that drop out periodically or when the ambient temperature is moved below 70°F or above 78°F. This occurrence appears to be related to intermittent connections which are expected to be found soon.

There has been a large amount of random noise observed on the "house ground" that can cause bit drop-out. The effect of this noise was significantly reduced by appropriately manipulating the grounding straps on the main frame. There is still occasional bit drop-out when the "house ground" noise becomes excessive, therefore grounding is still being studied.

The full decoder has operated for a maximum of 7 hours and typically 3 hours between failures. The time between failure will increase as intermittent solder connections on wafers are found and eliminated.

E. NINE-WORD MEMORY SUBSYSTEM

1. General

The nine-word Memory Subsystem was modified to operate with a 20-nsec cycle time. Memory planes, sense amplifier, digit driver, and word driver, etc., were fabricated to work with faster recovery so that the target cycle time could be obtained. Power supplies to individual circuits were changed to current source supplies by using resistor boards and potentiometers. Tests are now being conducted in the laboratory. This memory will hereafter be used to demonstrate the 24 bit lines required for the extensibility work.

The complete memory circuits are shown in Figure 3-13.

2. Subsystem Fabrication

a. Memory Plane and Word Driver

Not much change was made to the memory planes except that the word line viewers were mounted directly on the plane. The word switch and the first stage of read driver were temporarily omitted from the subsystem (they were fabricated and are awaiting tests), and a pulse generator was used to drive the second stage of the read driver directly.

b. Pre-amplifier, Sense Amplifier, and Digit Driver

A pre-amplifier was added between a digit line and a sense amplifier. The circuit layout of the pre-amplifier is the same as that of the 32-word subsystem except that the inductance is reduced to allow a faster recovery. The new versions of the sense amplifier and digit driver can be seen from Figure 3-13. In fabricating these circuits, special attention was paid to shortening the path between diodes, grounds,

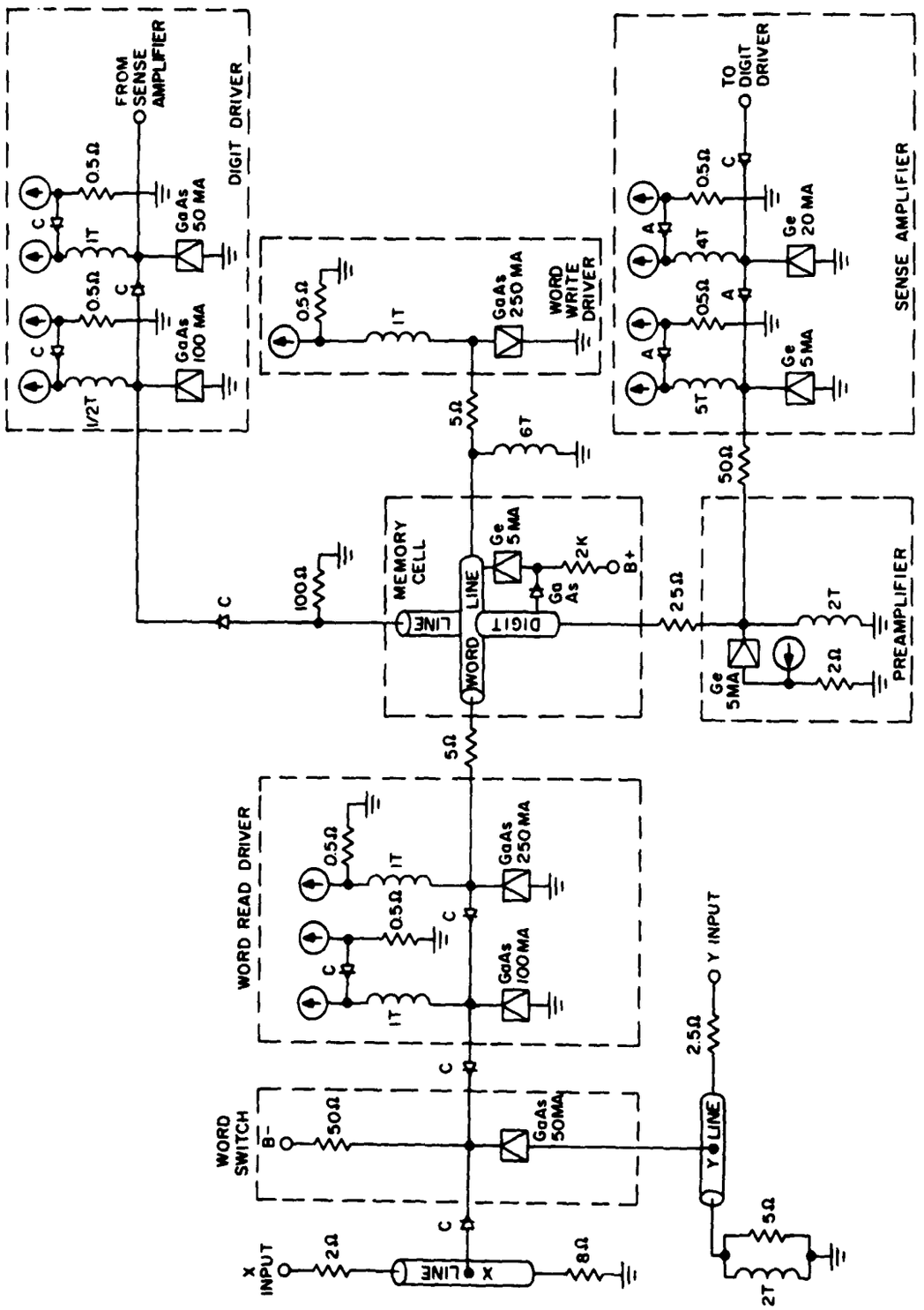


Figure 3-13. Circuits for 9-Word Memory

and circuits. As a result, the regeneration loop is about five inches shorter than that of the original layout. This was attained by moving the connecting brackets from the side to the bottom of wafers.

Digit drivers and sense amplifiers were raised from the bottom memory plane to the middle one so that more uniformity of regeneration loop length could be obtained from the three memory planes.

c. Resistor Boards and Potentiometer Panel

All the individual circuits are now tied to current source resistor boards which, in turn, are connected through a potentiometer panel to the common power supply.

3. Laboratory Results

The first phase of the new nine-word system put into operation was the word drivers. All diodes on the old system were replaced with in-spec units to allow operation from a common power supply. At present all the read and write word drivers are operating on all three planes. The power supply tolerance obtained on these circuits for complete operation was ± 5%.

The regeneration loops are now being put into operation. Each loop consists of a pre-amplifier, a sense amplifier and a digit driver. There are three such loops in the nine-word system. At present, the entire first plane is in operation. Any combination of "1"'s or "0"'s can be written into the memory cells on this plane. The cycle time for the regeneration loop is 20 nanoseconds. The tightest power supply tolerance occurs on the second stage of the sense amplifiers, a minimum tolerance of ± 3% overall. All other stages are at higher tolerances.

Work is now being done to install the second and third planes. Since these planes are serviced by the same sense amplifiers and digit drivers as the first plane, these should be easier to get into operation than the first plane.

F. EXTENSIBILITY MEMORY

1. Fabrication

The extensibility words are now complete and under test. By using closer component spacing, it has been possible to obtain a 24-bit word length using the same dimension as in the 5-bit word length of the 32-word subsystem. The plane consists of two word lines with a common memory bias line between them (Figures 3-9 and 3-14). All components have been attached by epoxy to the circuit since the close spacing did not make soldering desirable. Although more time is required to connect components using epoxy as compared with solder, loss of tunnel devices or resistors because of the heat required for soldering has been eliminated. Heat is required to cure the epoxy but this is relatively low (150°F) and does not endanger the components.

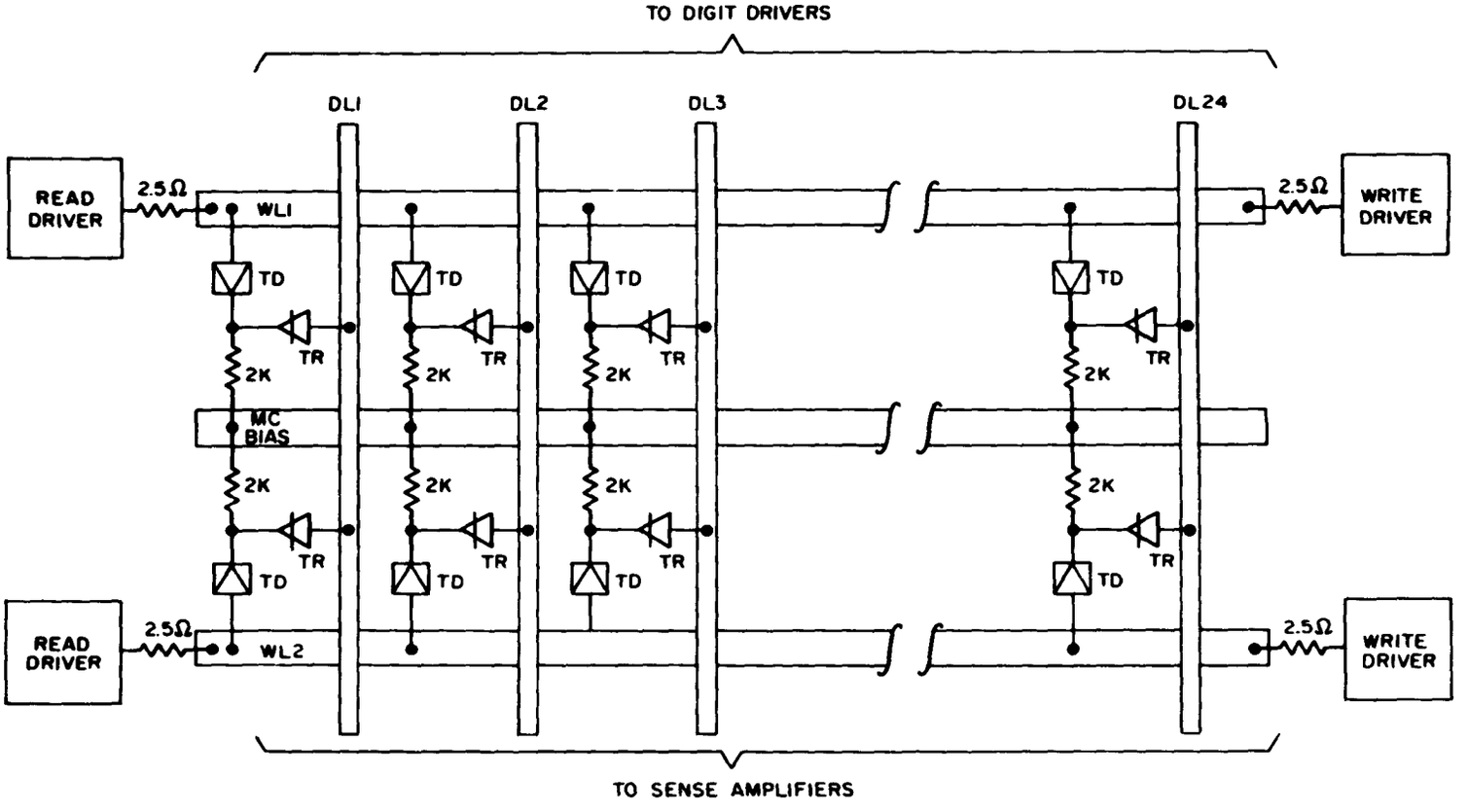


Figure 3-14. Extensibility Memory

A check of tunnel diodes after the epoxy operation showed they were all still within specifications although exact measurement is not possible since the component being viewed is shunted by other components. A layout of the 24 bits is shown schematically in Figure 3-14 and the approximate equivalent circuits when viewing individual tunnel diodes and rectifiers is shown in Figure 3-15.

2. Testing

The extensibility plane is being tested in the nine-word subsystem setup where it serves as one plane. Although there are 24 digit lines, only three can be sensed and regenerated at any one time. However, operation in this system demonstrates the ability to drive this length of word line as well as sense and regenerate the worst-case cell positions which are at the two ends of the word lines.

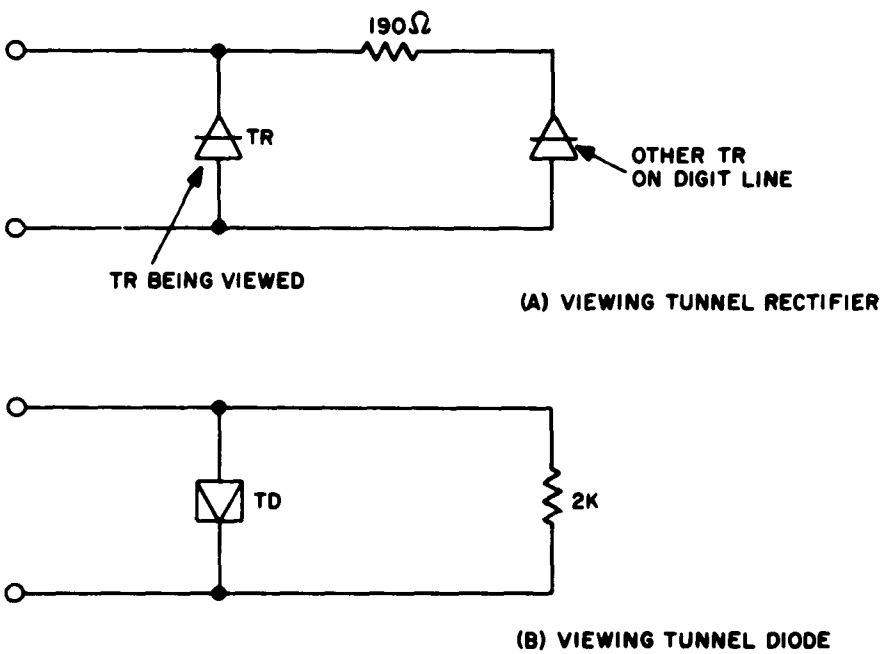


Figure 3-15. Equivalent Circuits for Extensibility Memory Cell